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Bachelor Thesis in Physics
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Calibration and Regulation of the Power Supply in the BrainScaleS System

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Abstract

The PowerIts main purpose is to measure and supply different voltages. In the Human Brain Projects BrainScaleS system, it delivers power to all system components. This thesis will provide a calibration of the PowerIt board as well as a regulation mechanism for its 1.8V power supplies.

Calibration of this board, will provide more accurate measurements, and allow for later regulation of its 1.8V outputs. First its circuitry will be examined and their behavior tested. Then the circuits can be calibrated. With these calibrations a method for regulating the main analog and digital power supplies will be implemented and verified on the Power wafer.

This thesis also contains the changes done to the PowerIt firmware while working on these tasks. The new firmware now has a new protocol for communication over a I^2C connection. It can be used for accessing any calibration parameter or on board measurement.

Zusammenfassung

Die Hauptaufgabe des PowerIts ist die Messung von, und Versorgung mit, verschiedenen Spannungen, die im BrainScaleS System des Humen Brain Projekts benötigt werden.

Diese Arbeit liefert eine Kalibration des PowerIt, sowie eine Methode zur Regelung der 1.8 V Spannungsausgänge. Zuerst werden dafür die verbauten Schaltungen untersucht, auf ihr verhalten getestet und daraus Kalibrationsdaten erfasst. Die spätere Regulierung der haupt Analog- und Digitalspannungen hängt dabei von der vorausgegangenen Kalibrierung ab.

Zusätzlich enthällt diese Arbeit die Änderungen, die an der Firmware vorgenommen worden sind, während diese Aufgaben bearbeitet wurden. Die neue Firmware enthällt nun ein neues Protokoll für die Kommunikation über einen I^2C-Bus. Dieses Protokoll kann dazu genutzt werden auf beliebige Kalibrationsdaten oder Messwerde zuzugreifen.

Contents

1 Introduction

This will be a short introduction to the BrainScaleS System and PowerIt.

1.1. The BrainScaleS System

The BrainScaleS wafer system which is visualized in figure 1.1, developed and used in the electronic visions group at Heidelberg University, is a neuromorphic hardware implementation [1]. On this hardware, mixed-signal ASICs, or also called HICANNs[1], implement a behavior similar to that of a neuron found in biological systems. These ASIC chips are placed on a silicon wafer, and grouped into packs of 8, called reticles. With these chips complex behaviors of biological systems can be simulated.

Focus of this thesis is part of the hardware implementation and only the following components will either be further examined or used later on:

- Control Units for Reticles, short CURE boards

  These boards control the power delivery mechanism for each of the 48 reticles.

- Analog Breakout boards, AnaB for short

  Provided by these boards are direct connections to reticle voltages, two per reticle. These are normally shared between all 8 reticles.

- and its power supply, called PowerIt.

[1] High Input Count Analog Neural Network

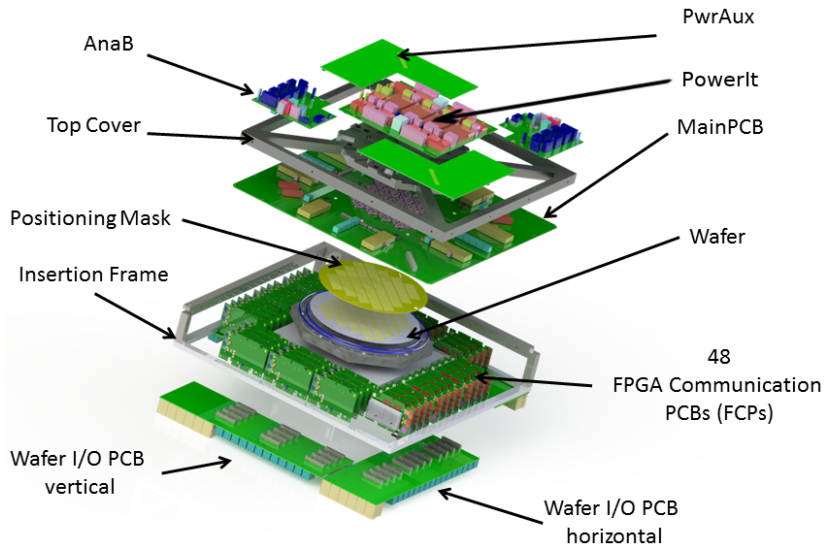

Figure 1.1.: The BrainScaleS wafer-scale hardware system, marked are the main components comprising a single wafer system. [2]

1.2. About the PowerIt Subsystem

The main subject of this thesis is the PowerIt board, photographed in figure 1.2. It functions as power supply inside of the wafer-scale system, described before, in which it provides e.g. the wafer with 1.8 V and the FPGAs with 9.6 V. Its maximum rated power draw is 2 kW. [3]
This PowerIt board has a integrated STM32 microcontroller[2] which runs a custom firmware based on ChibiOS [5]. For this thesis import ant is, that the chip runs at 169 MHz. Note that of its internal components mainly a 12bit ADC is used. It is clocked with the same internal frequency as the processor.

The PowerIt measures the following values via the STM32-internal ADC:

- input voltage and current
- 1.8 V output voltage and current each for analog and digital circuitry
- and the 9.6 V output voltage

which can then be used inside the firmware and read from devices via the I^2C connection. The external device can then get this information from the PowerIt to the BrainScaleS monitoring system.

The input voltage, nominal, is 48 V and therefore the input current should not exceed 41.7 A Additionally the 9.6 V are a set voltage obtained by the power supply modules[3] which divide the input voltage by 5. Lastly the 1.8 V output voltage is variable.

[2] STM32F405RGT [4]
[3] 5:1 Bus converter IB0xxE096T48xx, 500W each [?]

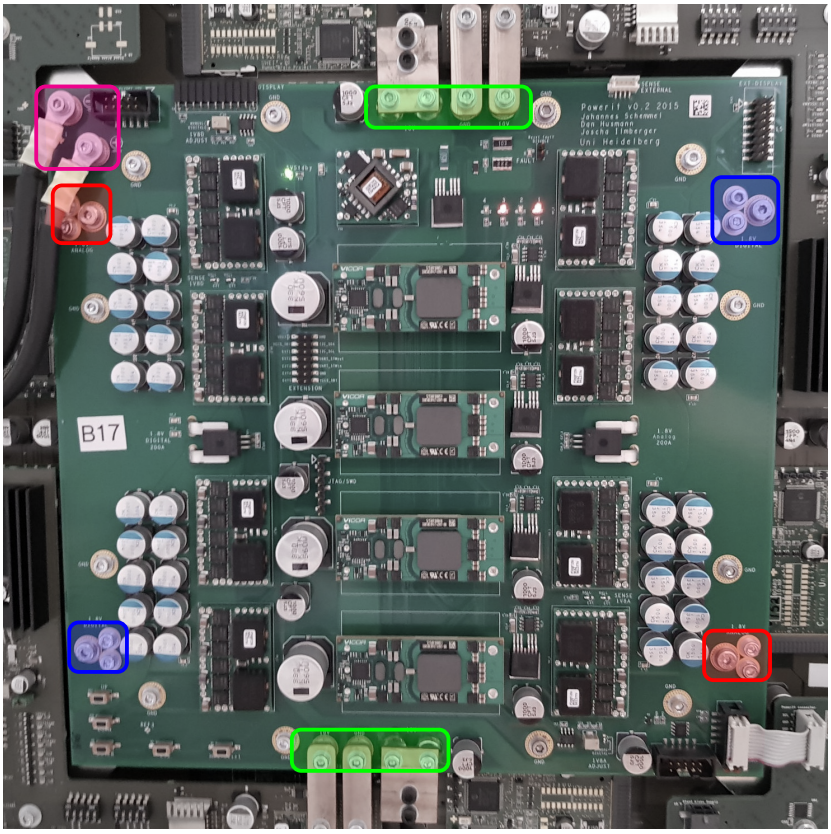

Figure 1.2.: Photograph of the PowerIt boards top view. It receives 48 V as input (magenta) and provides 9.6 V (green) and 1.8 V (analog: red, digital: blue)

1.3. Contents in Detail

The first goal was to be able to change the calibration parameters. An upgrade for the PowerIt firmware was added to accomodate for those values. This was accomplished with a virtual memory map, which maps every parameter to a specific location and all of them can be changed.

Calibrating the PowerIt was the next task. The calibration characterizes the voltage measuring circuits, whose voltages are either coming into or leaving the PowerIt. Additionally there are current measuring circuits for incoming current and both 1.8 V output currents. A reference voltage measurement was used to generate fitted polynomials. These polynomials coefficients are the calibration parameters used inside the PowerIt.

Taking these calibrations as basis, the 1.8 V power supplies' behavior through different current draws could be observed. A simple model was generated from these measurements and applied. Also inmplemented inside the firmware was a first iteration of that model which could now be tested.

2 Theory

This chapter will be discussing the principles used in the experiments. These will contain simplified circuits and their respective equations as well as component behavior, specified in their respective data sheets.

2.1. Hardware Component Behavior

Before discussing the experimental results it needs to be clear what circuitry is used in these experiments and what behavior we expect. Keeping in mind, that these are theoretical values and can be different from those found in actual hardware, as all given values will always be within some error.

Each of the three voltage regimes that can be observed on the PowerIt board, 48 V, 9.6 V and 1.8 V, has a voltage measurement circuit. In the cases of 48 V and 1.8 V there also exists a current measurement circuit. Additionally there is a temperature sensor built into the STM32 chip.

2.1.1. ADC Calibration

The measurements will be done by a STM32-internal ADC. A single ADC will be switching between all connected pins. This Behavior can be problematic in regards to measuring accurately. The reason for that is that the switching process requires the voltage to change within a given number of cycles (sample ticks). The measured voltage would be dependent on the previous value if this sample time is not big enough. The timing used to measure a single pin can be set from 3 up to 480 clock ticks.

2.1.2. 48V Input Voltage

The circuits for measuring input voltage and current are the most complex. For voltage measurement the circuit needs to

- divide our input voltage into a usable potential range, which is accomplished with a 1:240 voltage divider,
- decouple the input (48 V) from signal potential (3.3 V), with a full differential operation amplifier
- and amplify the voltage, to be in the STM32-Chips Voltage range of up to 3.3 V, with another amplifier, which also converts the differential into a single-ended signal.

The already implemented circuit can be seen in figure 2.1.

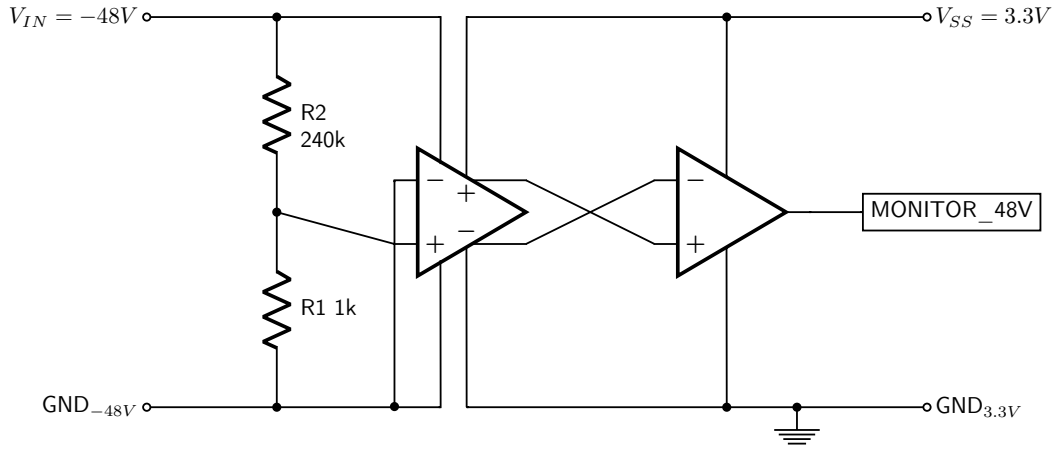

Figure 2.1.: Circuit for measuring the 48 V input voltage, consisting of input potential (left), two resistors as voltage divider, one fully differential isolation amplifier (left), one operational Amplifier (right), output voltage (right).

This circuit results in the following equation for calculating the input voltage from a pin voltage:

$$\begin{aligned} V_{\text{48V in}} \cdot \frac{R_1}{R_1 + R_2} \cdot r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}} &= V_{\text{MONITOR\_48V}} \\ \Leftrightarrow \quad \frac{V_{\text{MONITOR\_48V}}}{r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}}} \cdot \frac{R_1 + R_2}{R_1} &= V_{\text{48V in}} \end{aligned} \tag{2.1}$$

and the extremes, when assuming $(48.0 \pm 4.8)\,\text{V}$ are

$$V_{\text{MONITOR\_48V, min}} = 43.2\,\text{V} \cdot \frac{1}{240+1} \cdot 8 \cdot 1.1 \approx 1.6\,\text{V} \tag{2.2}$$

$$V_{\text{MONITOR\_48V, max}} = 52.8\,\text{V} \cdot \frac{1}{240+1} \cdot 8 \cdot 1.1 \approx 1.9\,\text{V} \tag{2.3}$$

The $(48.0 \pm 4.8)\,\text{V}$ range was chosen under the assumption of a maximum $10\,\%$ error, for the power supply. The ADCs 12bit resolution gives a maximum voltage resolution of $\approx 2\,\text{mV}$.

2.1.3. 48 V Input Current

The circuit has to satisfy the following constraints:

- use a shunt resistor, with minimal heat dissipation
- while still providing a good resolution within the STM32-Chips specifications

To accomplish that, the circuit is measuring the voltage over a $500\,\mu\Omega$ shunt Resistor, while a current is flowing. The shunt resistor also produces about 21 mW of heat at full current draw, which is easily dissipated. By Ohms Law that results in a linear proportionality between current

and the obtained voltage, which is then decoupled and amplified by a factor of 8. It is also then converted from a differential to single ended voltage, with a amplification factor of 1.1.

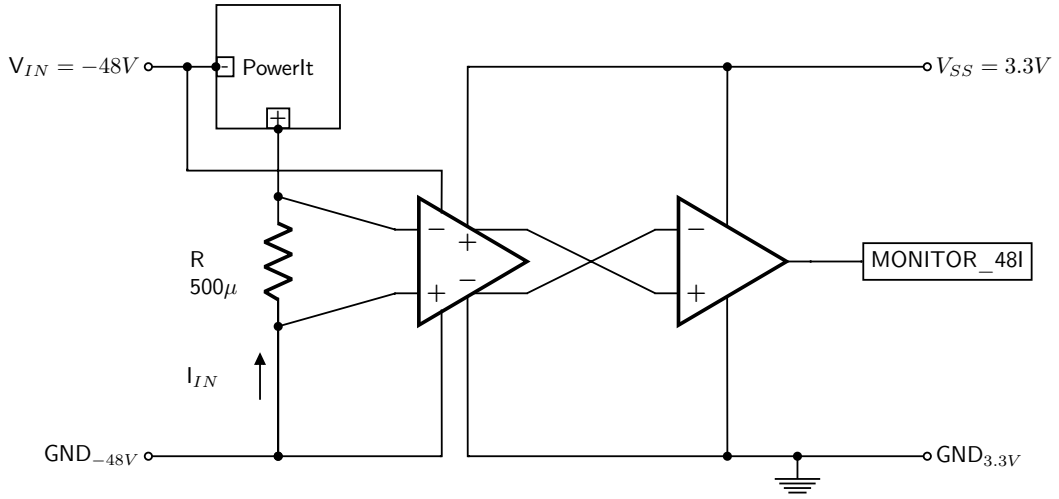

Figure 2.2.: Circuit for measuring the 48 V input current, consisting of PowerIt, one shunt-resistor, one full diff isolating Amplifier, one operational amplifier, output potential.

Here the same amplifiers as in subsection 2.1.2 are used and so we can apply the following equation for our input current:

$$\begin{aligned} & I_{\text{48V IN}} \cdot R_{\text{shunt}} \cdot r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}} = V_{\text{48I pin}} \\ \Leftrightarrow \quad & \frac{V_{\text{48I pin}}}{R_{\text{shunt}}} \cdot \frac{1}{r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}}} = I_{\text{48V IN}} \end{aligned} \tag{2.4}$$

The current range is from 0 A up to 41.7 A (= 2 kW / 48 V)and gives a resulting observable voltage range from 0 V to:

$$41.7\,\text{A} \cdot 500\,\mu\Omega \cdot 8 \cdot 1.1 \approx 185\,\text{mV} \tag{2.5}$$

This results in a maximum resolution of 0.18 A.

2.1.4. 9.6V Output Voltage

The measurement of 9.6 V output voltage circuit is quite a bit simpler. This circuit consists of a 1:3 voltage divider.

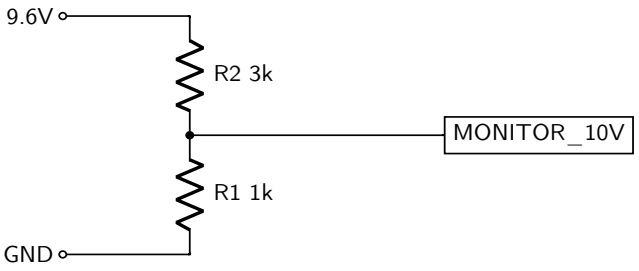

Figure 2.3.: Circuit for measuring 9.6V output voltage. Consisting of a voltage divider with 1:3 ratio, input voltage (left) and output voltage (right)

To describe that circuit the following equation can be used:

$$\frac{V_{\text{9.6V IN}} \cdot R_1}{R_1 + R_2} = V_{\text{MONITOR\_10V}} \tag{2.6}$$

$$\Leftrightarrow \frac{V_{\text{MONITOR\_10V}}}{R_1} \cdot (R_1 + R_2) = V_{\text{9.6V IN}} \tag{2.7}$$

With the given voltage range of the input voltage from 43.2 V to 52.8 V the observable voltage range for this circuit is from 8.64 V to 10.56 V. And with the 12bit ADC that gives a maximum resolution of 3.2 mV

2.1.5. 1.8V Output Voltage

This voltage is measured directly with the STM32-Chip.

Until now the voltages and currents could only be measured, now the mechanism for setting a resulting voltage at the 1.8 V terminals is changeable. The circuit for generating 1.8 V can be seen in figure 2.4. It consists of a power module and the three resistors R_{series}, $R_{parallel}$ and R_{pot}. The resistances set the output to a given voltage of around 1.8 V. Based on R_{pot} this voltage is varied, because this resistance is settable via a digital potentiometer[1].

[1] MCP4152 digital potentiometer [6]

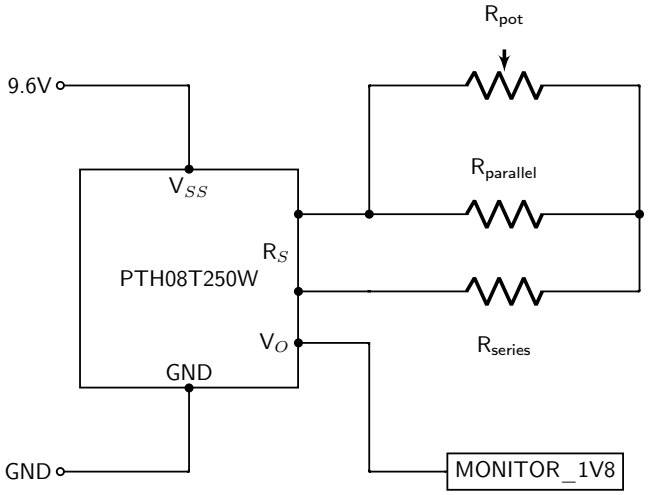

Figure 2.4.: Schema of a 1.8V supply circuit. It features a DC-DC Converter, a resistor chain, supply voltage (left) and resulting voltage (V_O).

The in figure 2.4 used 1.8 V converter has a characteristic output voltage formula [7], written in equation 2.10. The in this circuit used 10 kΩ potentiometer is linear.

Therefore equations 2.8, 2.9 and 2.10 describe the circuit.

$$R_{\text{pot}} = P_{\text{val}} \frac{10\,\text{k}\Omega}{256} \tag{2.8}$$

$$\begin{aligned} R_S &= \left(\frac{1}{R_{\text{pot}}} + \frac{1}{R_{\text{parallel}}} \right)^{-1} + R_{\text{series}} \\ &= \frac{R_{\text{pot}} \cdot R_{\text{parallel}}}{R_{\text{pot}} + R_{\text{parallel}}} + R_{\text{series}} \end{aligned} \tag{2.9}$$

$$V_{\text{MONITOR\_1V8}} = \frac{30.1\,\text{k}\Omega}{R_S + 6.49\,\text{k}\Omega} \cdot 0.7\,\text{V} + 0.7\,\text{V} \tag{2.10}$$

Visualizing the equation 2.9 results in figure 2.5, in which the limits of this circuit are visible.

$$V_{\text{MONITOR\_1V8, min}} \approx 1.6\,\text{V} \tag{2.11}$$

$$V_{\text{MONITOR\_1V8, max}} \approx 2.0\,\text{V} \tag{2.12}$$

And these extremes will be a limiting factor later on. Also with the 12bit ADC that results in a maximum resolution of $\approx$1 mV.

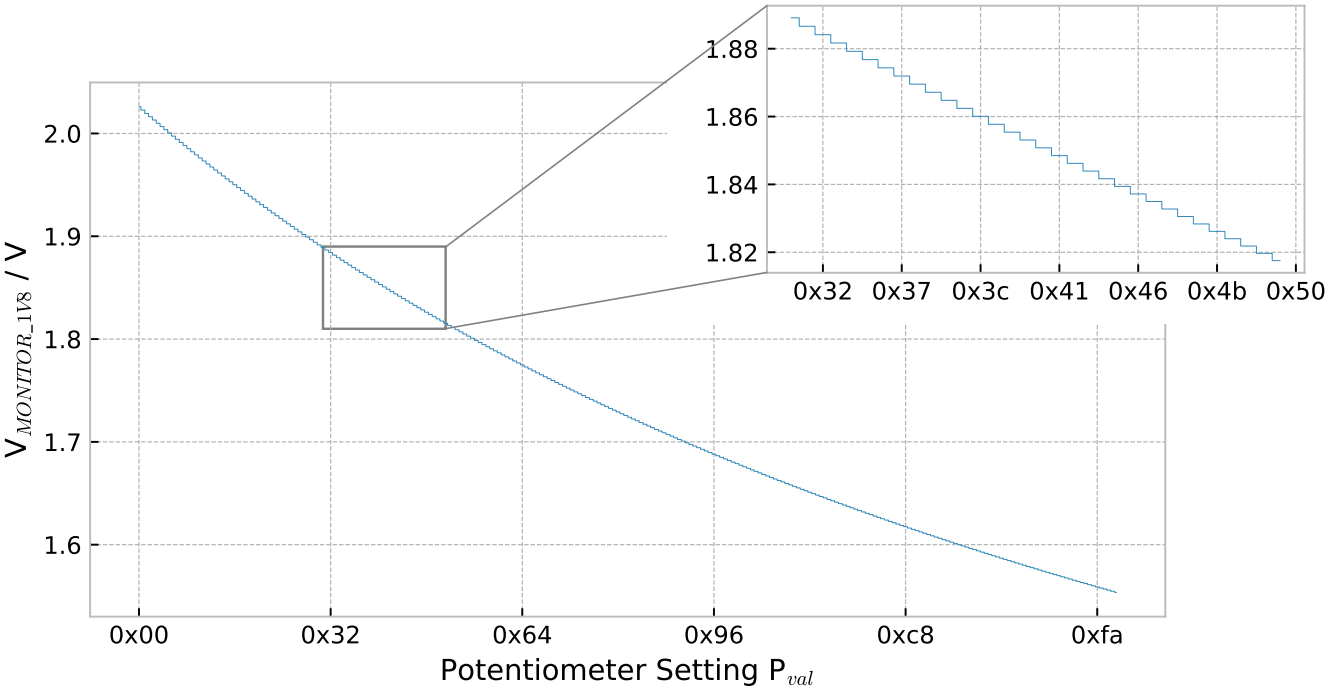

Figure 2.5.: Expected behavior curve of 1.8V output voltage vs potentiometer setting. Shown is the complete range of possible settings and their resulting voltage. The zoomed in partial view shows that because the setting can only be of integer value any resulting values are also discrete. A single step can increase the voltage by somewhere between 1.1 mV and 3.3 mV

2.1.6. 1.8V Output Current

The outgoing current over 1.8V is measured by a hall sensor, which outputs a voltage to be measured. Each connection (digital and analog) has this sensor in series to its load.

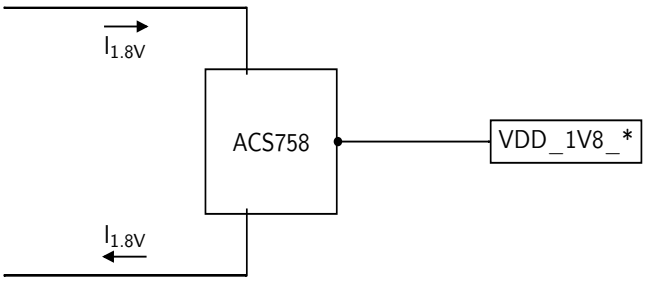

Figure 2.6.: Circuit for measuring 1.8V current. It features a ACS758 hall sensor, input current (left) and output voltage (right)

The hall sensor is rated for a maximum constant current draw of 200 A, and features the following behavior:

$$I_{1.8\text{V, in}} \cdot 0.004\,\text{V}\,\text{A}^{-1} + 0.12\,\text{V} = V_{\text{MONITOR\_1I8}} \tag{2.13}$$

By applying the limits of 0 A and 200 A, the following voltage range can be observed:

$$0\,\text{A} \cdot 0.004\,\text{V}\,\text{A}^{-1} + 0.12\,\text{V} = 120\,\text{mV} \tag{2.14}$$

$$200\,\text{A} \cdot 0.004\,\text{V}\,\text{A}^{-1} + 0.12\,\text{V} = 1040\,\text{mV} \tag{2.15}$$

These values and the used 12bit ADCs gives a maximum resolution of around 0.2 A

2.2. 1.8V Output Regulation

The method for regulating the 1.8 V output voltage consists of two parts.

First the voltage, which is wanted at the output terminal and second the corresponding potentiometer setting to use for that voltage, on the other hand, to calculate the voltage to output, it is necessary to classify the connections between the PowerIts output terminals and reticles.

2.2.1. Potentiometer Mapping

Combining Equations 2.8, 2.9, and 2.10, we gather equation 2.16. This equation maps a given output voltage to a corresponding potentiometer setting (reverse to figure 2.5).

$$P_{\text{val}} = \frac{R_{\text{par}} \left[\left(\frac{0.7V \cdot 30.1k\Omega}{V_O - 0.7V} - 6.49k\Omega \right) - R_{\text{ser}} \right]}{R_{\text{par}} + \left(\frac{0.7V \cdot 30.1k\Omega}{V_O - 0.7V} - 6.49k\Omega \right) - R_{\text{ser}}} \cdot \frac{256}{10k\Omega} \tag{2.16}$$

2.2.2. Power Wafer

To test the 1.8 V regulation the so called PowerWafer is going to be used. Its reticles can be controlled via the CURE board, similar to HICANN wafers, which are used in BrainScaleS, but the Power Wafer is different, as it cannot be used for any neuromorphic computation. Its internals are ohmic resistors, which provide a maximum power draw per reticle of what is possible inside a usable wafer module.

It has the same layout as its system counterparts and each of the 48 reticles can be accessed digitally, as well as electrically.

And like its system counterparts it is placed on a MainPCB (see figure 2.7). All CURE boards connect to it and control the PowerFETs, as well as provide voltage readout from each reticle.

Also on the MainPCB are the AnaB boards. Note that here lies another specialization of the PowerWafer. All reticles' analog and digital 1.8 V lines are connected directly to pins on the analog readout boards [8]. There it is possible to access a voltage, which is measured after the load resistors in figure 2.8 (after [1])

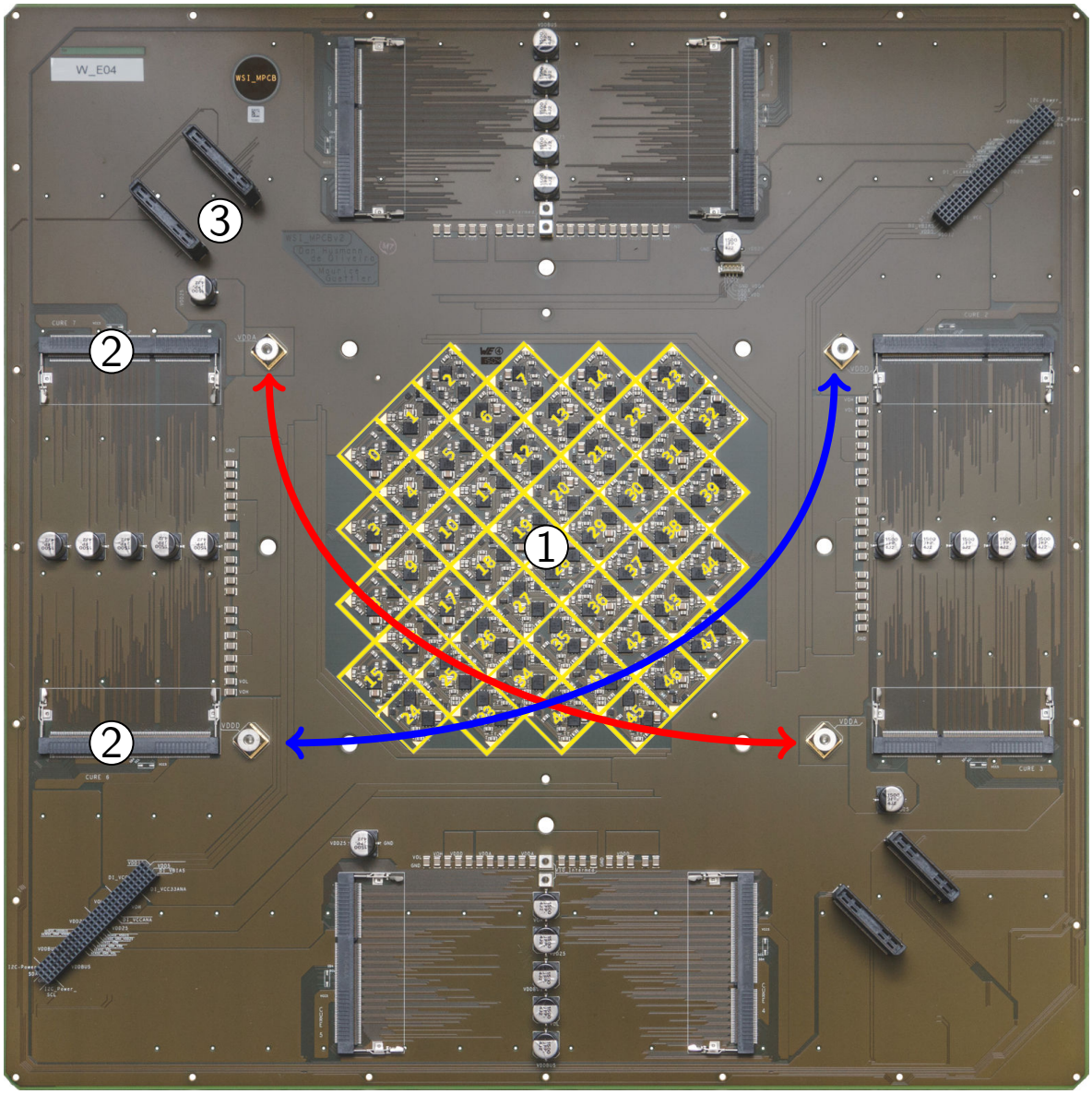

Figure 2.7.: A photograph of the top of the MainPCB (courtesy of Maurice Güttler [1]). The board has a length and width of 43cm. Visible in the center are the PowerFETs (Field Effect Transistors) (1) which switch the power supply of each reticle. These are controlled via the CURE boards (2). In yellow the corresponding Reticle and its position is marked. All 48 Reticles are shown. A single reticle has a width of 20.0482 mm and height of 20.145 mm, with additional space in between reticles of 420 µm horizontally and 250 µm vertically [1]. The top-left and bottom right corner connectors (3) are for the AnaB boards. The main supply voltages V_{DDA} (red) and V_{DDD} (blue) are generated on the PowerIt and inserted at the marked screw connections.

2.2.3. Simple Wafer Resistance Model (SWRM)

When powering any reticle on a wafer system, the voltage on the PowerIt side is set to about 1.9 V. This then results in the reticles receiving around 1.8 V. Additionally when running experiments on a HICANN wafer, the current draw results in a drop of this received voltage. This behavior is the result of a resistance between power supply and reticles.

To describe the resistances on such a wafer module, a model can be used. This model combines all resistances introduced through any connection point between supply terminal (copper pad on PowerIt) and PowerFET into R_0. It also represents the connection between FET and reticle as another resistor R_1. For this simple model the circuit in figure 2.8 is used.

This naive model will be referenced as SWRM (Simple Wafer Resistance Model) from here.

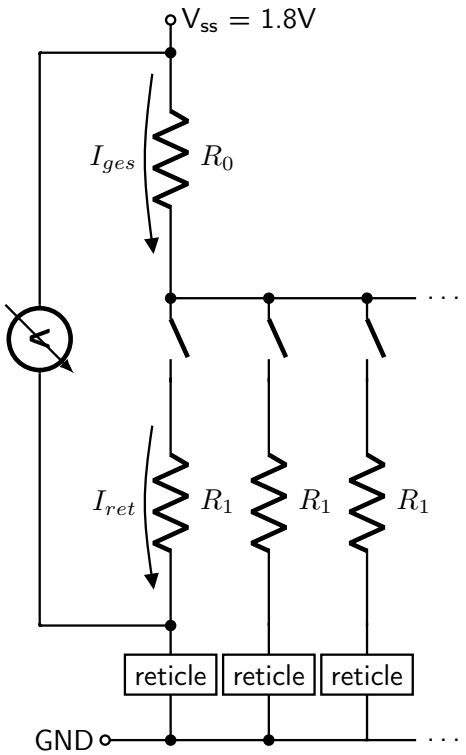

Figure 2.8.: SWRM circuit containing the to measure resistances and their currents. R_0 describes the resistance of a connection between the PowerIt output and up to the FET (depicted as switch), while R_1 is a resistance between FET and Reticles. The measurement is done between on the PowerIt and pins on a AnaB.

The SWRM circuit consists of two fixed resistance values and their respective currents as approximations of a real world system. It assumes that the connection to the nearest voltage connector is equal (electrically) for all reticles.

In the SWRM, the current flowing through R_1 will be either 0 or a constant current I_{ret}. And the current through R_0 will change depending on the number of reticles that are powered n_{ret}

$$I_{ges} = n_{ret} \cdot I_{ret} \tag{2.17}$$

Therefore the voltage drop V_{drop} as measured by a voltmeter (connected as in figure 2.8) can be described with equation 2.18

$$\begin{aligned} V_{\text{drop}} &= V_{R_1} + V_{R_0} \\ &= R_1 \cdot I_{\text{ret}} + R_0 \cdot I_{\text{ges}} \\ &= I_{\text{ret}} \cdot (R_1 + R_0 \cdot n_{\text{ret}}) \end{aligned} \tag{2.18}$$

$$V_{\text{drop}} = V_O - V_{\text{off}} \tag{2.19}$$

$$\Rightarrow V_O = I_{\text{ret}} \cdot (R_1 + R_0 \cdot n_{\text{ret}}) + V_{\text{off}} \tag{2.20}$$

Equations 2.19 and 2.20 reference the desired voltage at reticle level Voff and the voltage at a PowerIt terminal V_O.

3 Experiments

Now that the theoretical model is complete, experiments were done and the model checked. The results of these experiments are usable for either voltage or current calibration.

3.1. Experimental Setup

The first setup was used during the calibration phase, while the second setup was used for creating the regulation model.

3.1.1. Calibration Setup

To calibrate a PowerIt, a setup is required that can sweep the input voltage, as well as draw different currents from the PowerIt (see figure 3.1). For that a setup with a bench power supply an electronic load and an external voltmeter are used. Additionally a STM32-Discovery board and a RaspberryPi microcomputer were connected to flash new firmware onto the PowerIt.

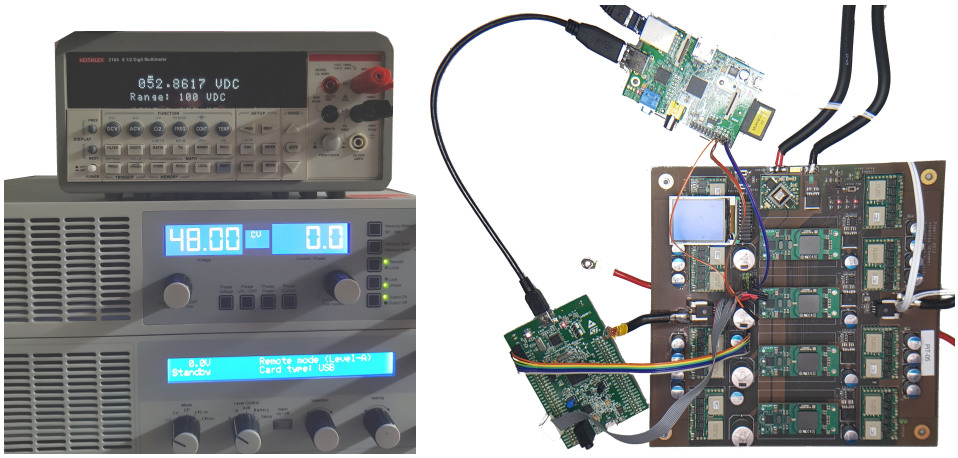

Figure 3.1.: Photographs of the first experimental setup. On the left side visible are a Keithley K2100 voltmeter (top), a Elektro-Automatik PS8080 bench power supply (middle) and EL9080 electronic load (bottom). On the right side visible are a PowerIt with connected STM32-Discovery board (left), and Raspberry PI (top). Also in the picture is the power supply connection (cables at top of PowerIt).

To now calibrate the board the bench supply could be controlled, to sweep through a voltage range, or in a similar fashion the electronic load could sweep through different current draw scenarios.

3.1.2. Power Wafer Setup

To obtain the required measurements for creating a regulation model the second setup was used (figure 3.2). These required measurements are the calculation of I_{ret}, R_0 and R_1 of equation 2.20.

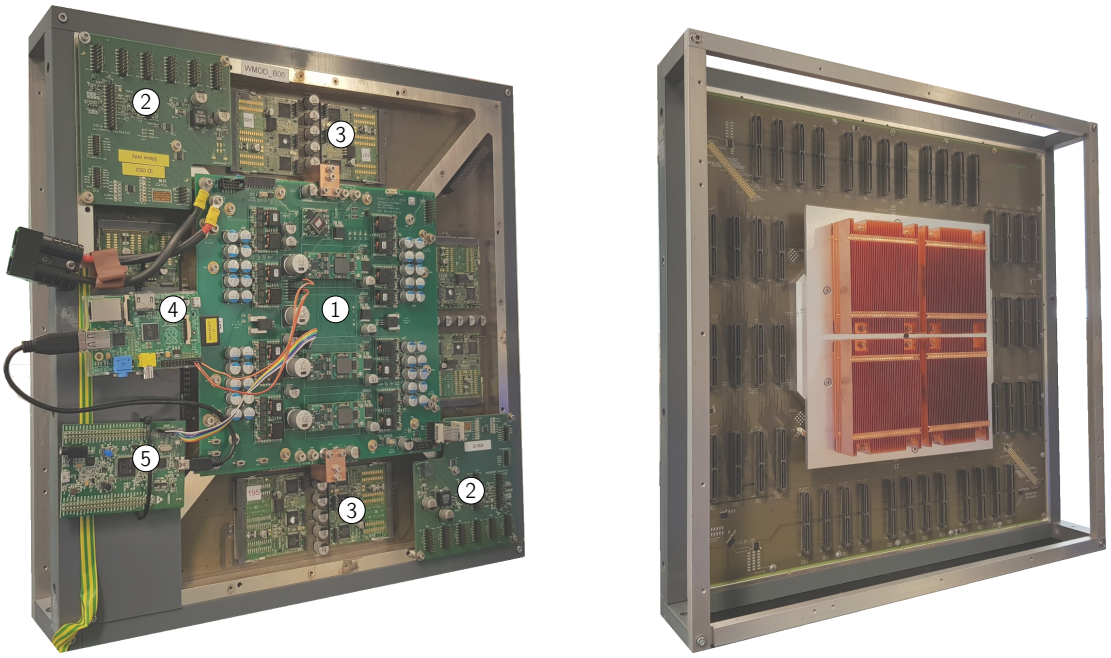

Figure 3.2.: Photographs of the second experimental setup. In this setup the wafer system assembly was used. This module has a height and length of 50cm and a width of 15cm. The left side shows the back side of the assembly. Here are the PowerIt (1), CURE (3) and AnaB (2) boards mounted, as well as a RaspberryPi (4) and a STM32-Discovery (5). The right side shows the empty front side of the MainPCB and the wafer heat sink.

This setup is similar to a BrainScaleS wafer module as it exists inside the system, but in contrast to these systems there are no FPGAs, AuxPwr or FCP boards (reference [1],fig 2.2). The MainPCB has the PowerWafer attached and is also connected to 8 CURE boards, 2 AnaBs and a PowerIt.

3.2. Characterization

The first experiments to run are the characterization of hardware behavior. These will then result in a PowerIt calibration, which later then can be used as basis for creating a regulation method.

For the complete calibration process the calibration setup was used.

3.2.1. Sampling Time

First up was selecting an optimal sample tick number.

In this case the uncalibrated measurement of input voltage was taken as example, and repeated with each of the possible 8 settings.

In addition a voltage measurement was taken with an external voltmeter[1]. The voltmeter was

[1] Keithley 2100

connected to the 48 V input voltage terminal. The difference from the supplied Voltage, set with the external power supply, was then calculated. In figure 3.3 these calculated values are plotted. The in figure 3.3 contained absolute error of the voltmeter is not 0 but signifficantly different from the power supply voltage. Therefore from here on the reference voltages were taken with the external voltmeter, if possible. This avoids added uncertainty introduced by the power supply.

Also shown are the calculated gain errors, in case of all 8 settings. Important to note is the relative error in only one case not usable. Here the `cycleTime`-setting was set to 0 and therefore the smallest available sampling time of 3 ticks was chosen. This result excludes 0 as a possible value to use. All other measurements are within error margin of each other, and because a smaller time frame is preferred, the best value to use is 1. This results in a sample time of 15 Ticks or 77 ns per pin.

3.2.2. Voltages

Now that a sample time is chosen, it is possible to proceed with the voltage calibration measurements. Note, that measurements can be less accurate, the more components are contained in their respective measurement circuit. The reason for that is, that small errors can accumulate and in e.g. the case of 48V's be amplified by a factor of 8.

48V Input

In this setup the voltmeter is connected to the positive and negative input voltage terminals.

When looking at calibrating the input voltage (figure 3.4), we can clearly see a relatively constant offset of $\approx$1V. This is most likely the result of a offset voltage introduced behind the secondary amplifier. In figure 3.4 a polynomial fit of 2nd degree[2] is done and its coefficients extracted (code 1, line 9). These coefficients not only show an offset, but also some deviation in the incline and curve from the default values (code 2).

[2] A Fit of second degree will be used in the complete calibration process

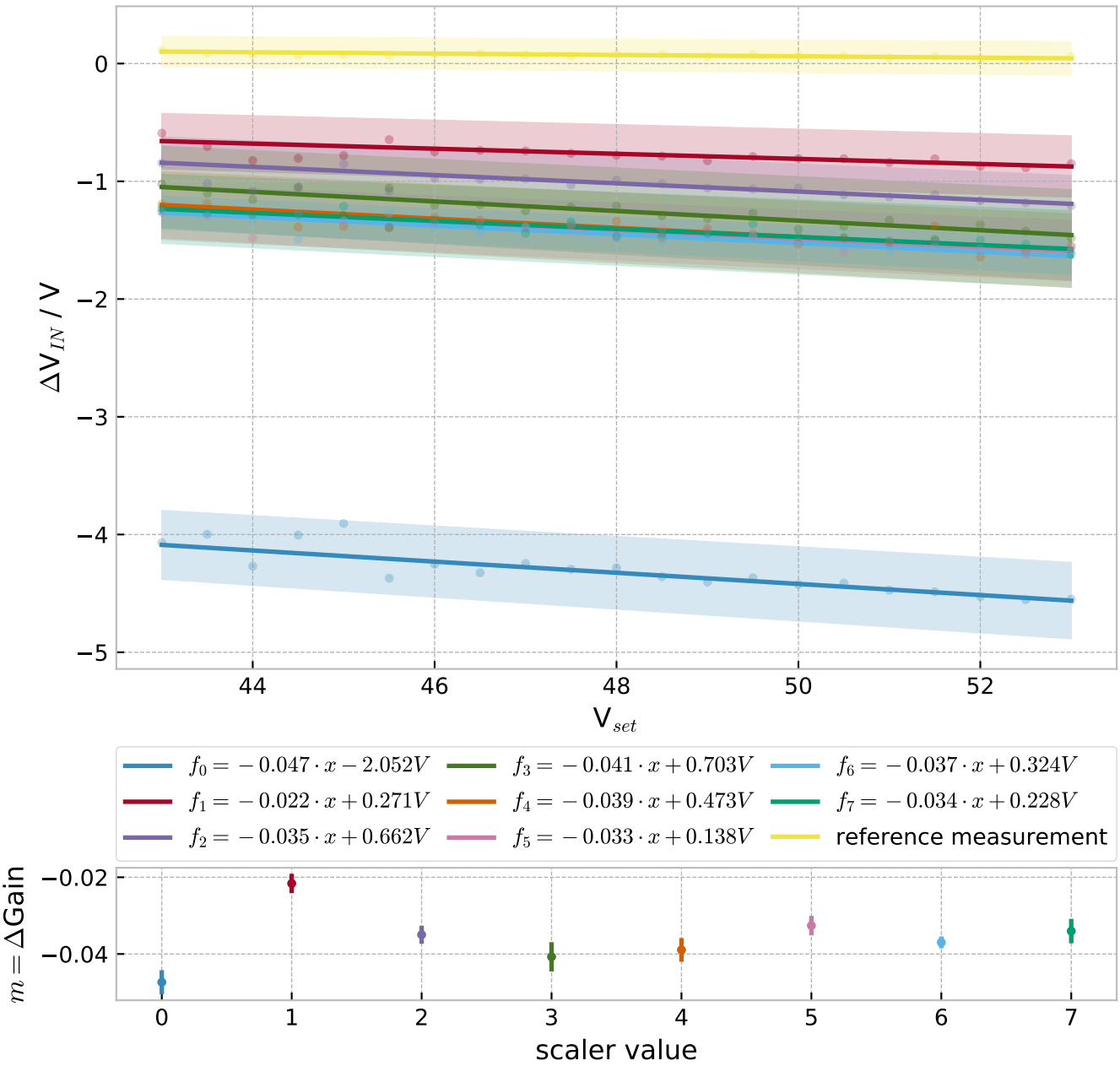

Figure 3.3.: Top: input voltage difference vs set voltage for different possible sampleTick values. Bottom: gain error of the linear fitted curves vs set scaler value.

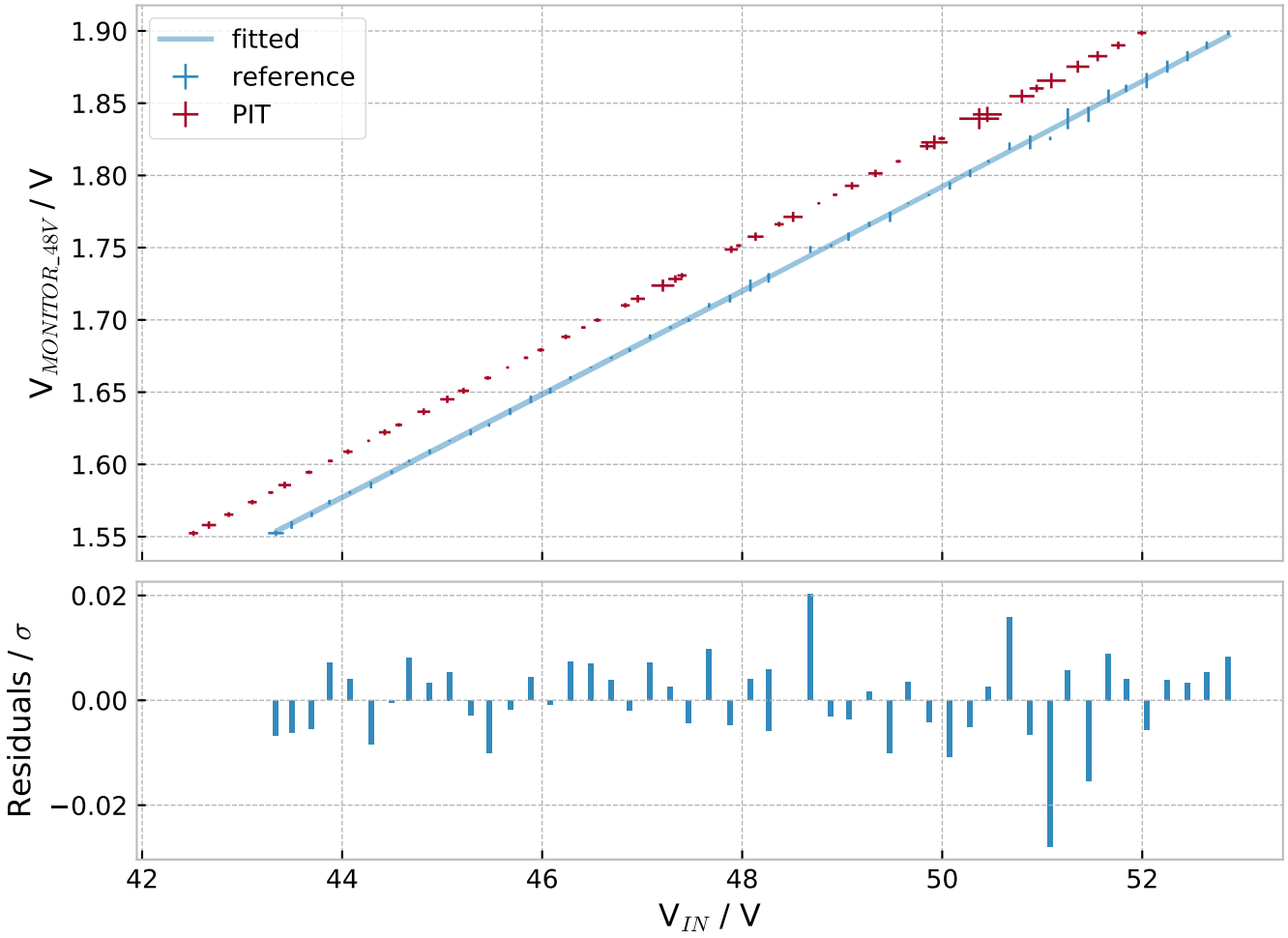

Figure 3.4.: Calibration of 48 V input voltage. Plotted are measured and reference vs the calculated pin voltage. The calibration sweeps from 43.2 V to 52.8 V. The fit is of second degree and its inverse are the to use calibration coefficients. (fit:$(7.15 \pm 3.59) \times 10^{-5}\,\mathrm{V}^{-1} V_{\mathrm{IN}}^2 + (2.92 \pm 0.35) \times 10^{-2} V_{\mathrm{IN}} + (1.56 \pm 0.83) \times 10^{-1}\,\mathrm{V} = V_{\mathrm{MONITOR\_48V}}$)

9.6V Output

For this setup the voltmeter was connected to a PowerIt `GND` and `10V` pad.

The 9.6V calibration, shows a slight difference between internal values and the reference measurement. This results in a list of coefficients (see code 1, line 7), very similar to those set in the theoretical defaults (see code 2).

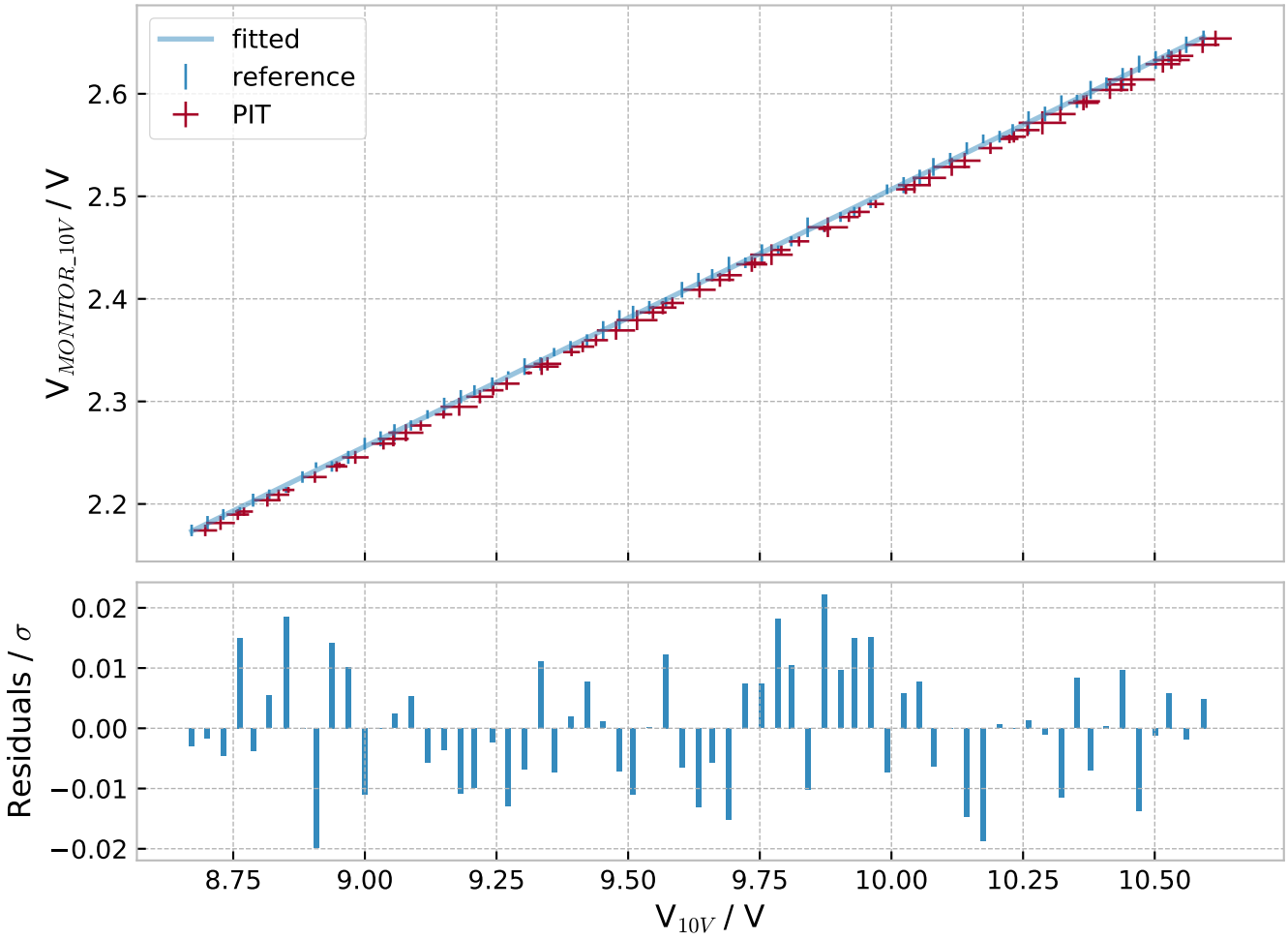

Figure 3.5.: Calibration of 9.6 V input voltage. Plotted are measured and reference vs the calculated pin voltage. The Calibration sweeps from 43.2 V to 52.8 V, and the supply modules divide that into 8.64 V to 10.56 V. The fit is of second degree and its inverse are the to use calibration coefficients. (fit:$(-0.10 \pm 1.23) \times 10^{-3}\,\mathrm{V}^{-1} V_{10\mathrm{V}}^2 + (2.53 \pm 0.24) \times 10^{-1} V_{10\mathrm{V}} + = V_{\mathrm{MONITOR\_10V}}$)

This small difference is explained by the simple voltage division used as our circuitry, and no amplification, like for the input voltage circuit. The residuals also show no systematic errors.

1.8V Output

The last voltage to calibrate is divided into two domains, one for supplying the analog, and one for the digital side of the wafer circuitry. Each deliver between 1.549 V and 2.022 V and both are settable by their respective circuit (both as in figure 2.4).

And for each measurement the voltmeter was either connected to PowerIt `GND` and `1.8V analog` or `1.8V digital` pins.

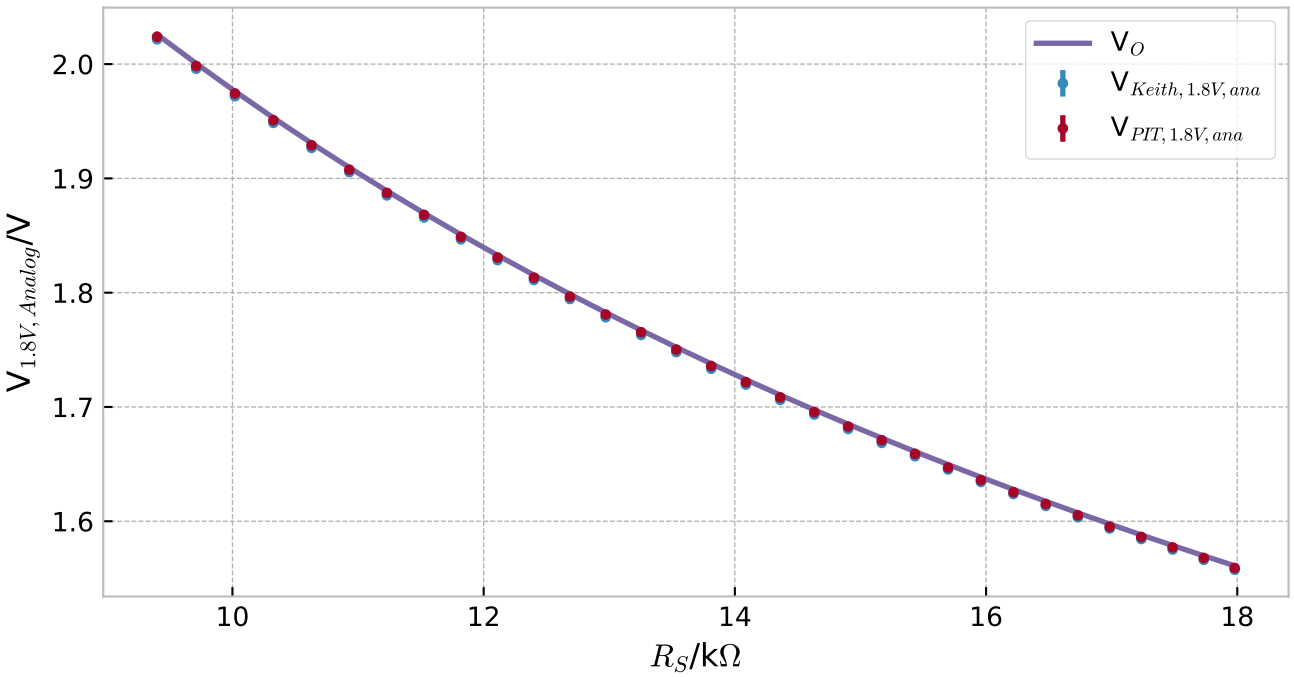

Figure 3.6.: Calibration of analog 1.8V output voltage, plotted are external measurement and internal values vs set resistance R_S at the voltage module.

Visualized in figure 3.6 is the analog domains calibration, showing nearly no difference in board and reference measurements. Mostly due to direct connection between created voltage and the STM-Chips pin.

3.2.3. Currents

With now calibrated voltages, the next step is to observe the behavior of the current measuring circuits. Note that the 9.6V output does in fact not have a include circuit for measuring its current draw, and that this number will be obtainable from all other (calibrated) measurements.

48V Input

This experiment will calibrate the 48V input current. The setup consists of connecting the electric load to `GND` and `10V` pins. In it the current drawn by the PowerIt sweeps over a range from 0 A to 20 A.

In figure 3.7 quite a gap between observed and measured values can be seen. This is most likely a gain error, which would result in a error in m_2, as observed. And the fitted curve has the following parameters:

$$
\begin{aligned}
V_{\text{MONITOR\_48I}} &= m_0 + m_1 \cdot I_{\text{IN}} + m_2 \cdot I_{\text{IN}}^2 \qquad (3.1)\\
m_0 &= (2.64 \pm 1.01) \times 10^{-3}\,\text{V}\\
m_1 &= (5.63 \pm 0.25) \times 10^{-3}\,\text{V A}^{-1}\\
m_2 &= (1.36 \pm 0.13) \times 10^{-4}\,\text{V A}^{-2}
\end{aligned}
$$

from which the inverse will be used for calibration inside the PowerIt.

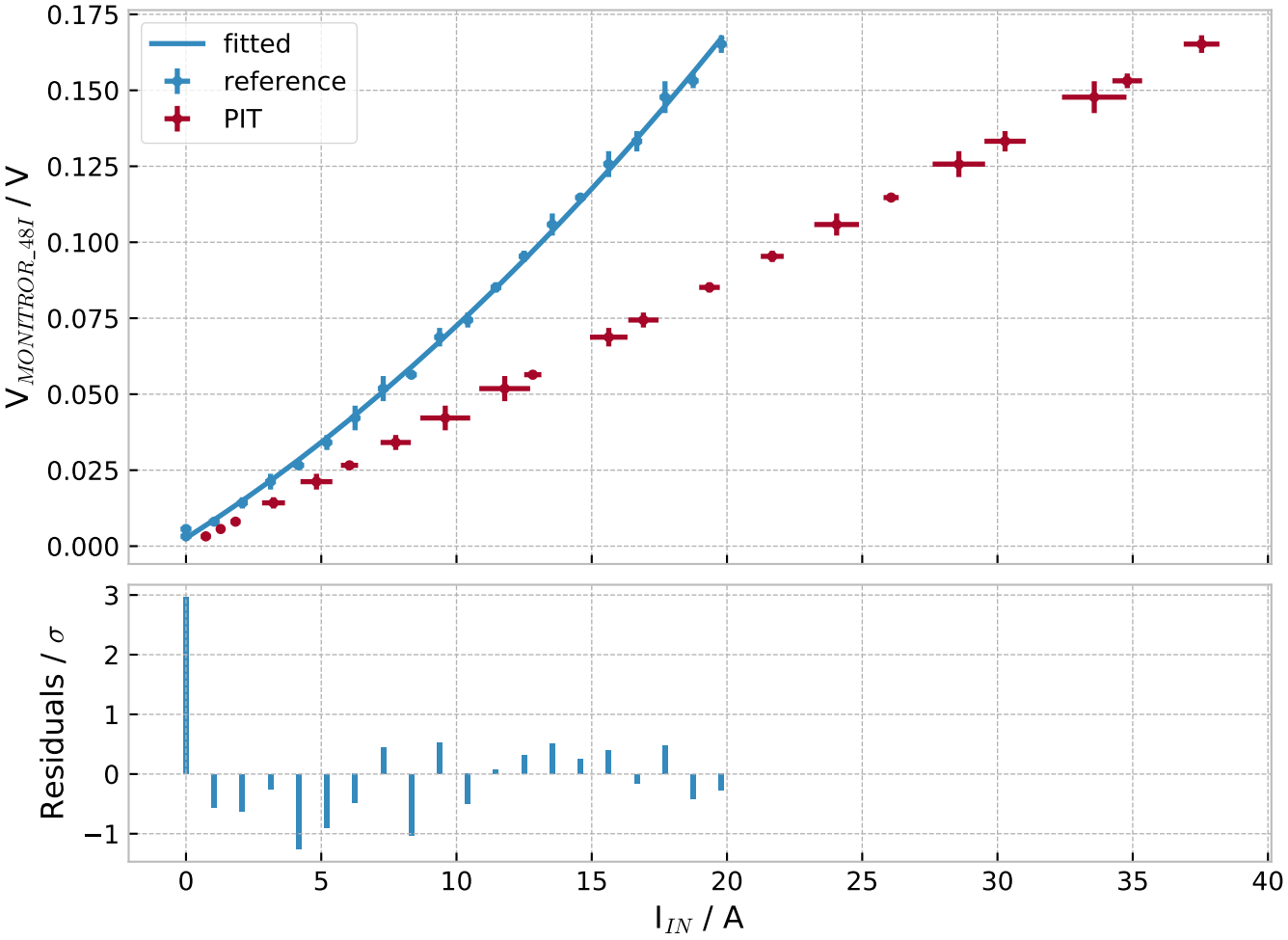

Figure 3.7.: Calibration of 48 V input current. Plotted are measured and reference current vs the calculated pin voltage. The Calibration sweeps over 0 A to 20 A. The fit is of second degree and its inverse are the to use calibration coefficients.

1.8V Output

For the calibration experiment of both 1.8V output currents, the current draw ranges from 0 A to 90 A. The electric load was connected to a `GND` and `1.8V analog` or `1.8V digital` pin

depending on the measurement. Observed were the values in figure 3.8. Visible is a different incline of internal measurement and reference.

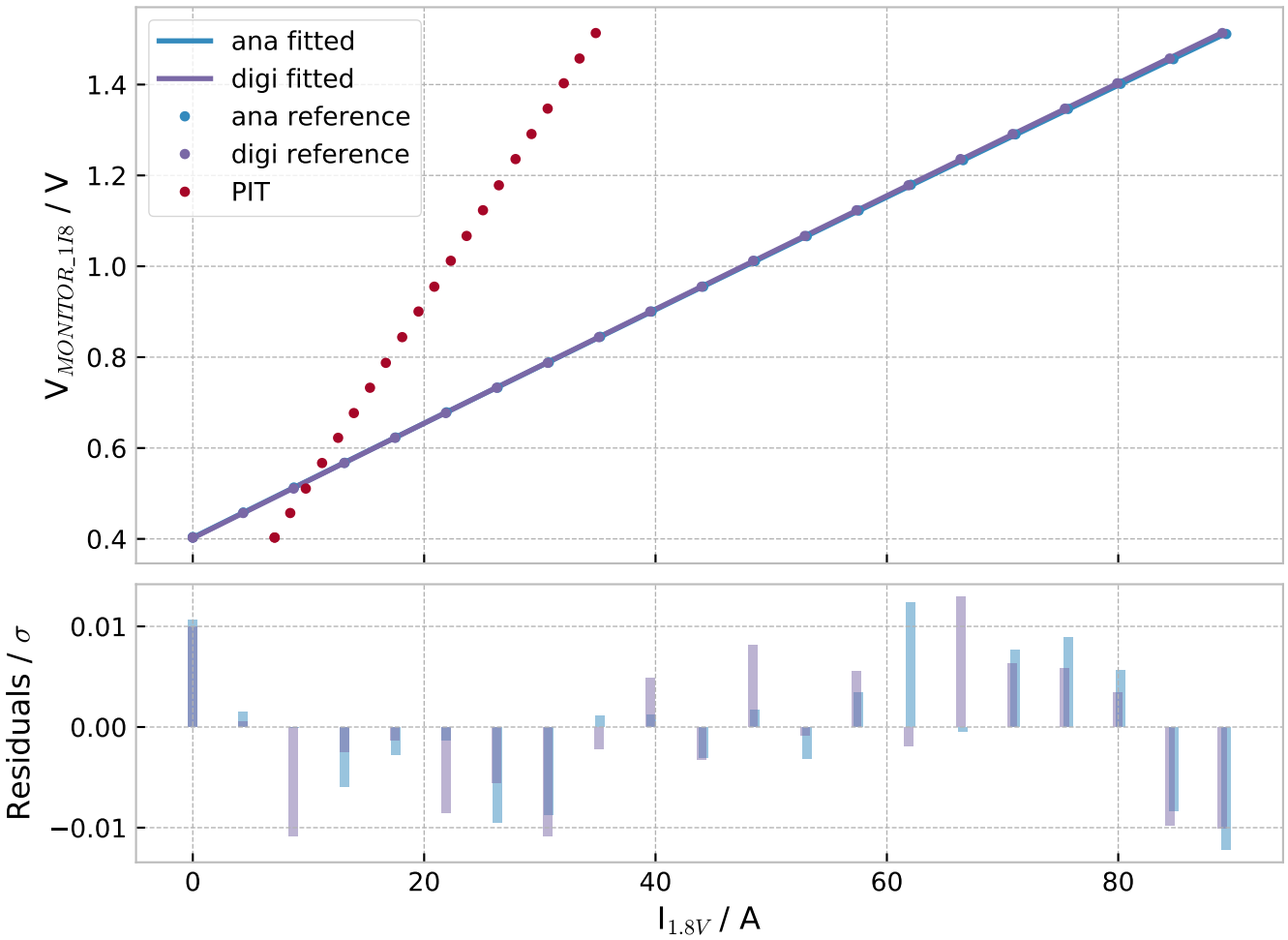

Figure 3.8.: Calibration of 1.8 V output current for both digital and analog. Plotted are measured and reference current vs the calculated pin voltage. The Calibration sweeps over 0 A to 90 A. The fits are of second degree and their inverse are the to use calibration coefficients.

The fitted curve for the analog side were:

$$V_{\text{MONITOR\_1I8\_ANA}} = m_0 + m_1 \cdot I_{\text{1.8V, ana}} + m_2 \cdot I^2_{\text{1.8V, ana}} \tag{3.2}$$
$$m_0 = (4.03 \pm 0.00) \times 10^{-1}\,\text{V}$$
$$m_1 = (1.26 \pm 0.00) \times 10^{-2}$$
$$m_2 = (-2.33 \pm 0.27) \times 10^{-6}\,\text{V}^{-1}$$

, while the digital side had quite similar values of:

$$V_{\text{MONITOR\_1I8\_DIGI}} = m_0 + m_1 \cdot I_{\text{1.8V, digi}} + m_2 \cdot I^2_{\text{1.8V, digi}} \tag{3.3}$$
$$m_0 = (4.02 \pm 0.01) \times 10^{-1}\,\text{V}$$
$$m_1 = (1.27 \pm 0.00) \times 10^{-2}$$
$$m_2 = (-1.90 \pm 0.31) \times 10^{-6}\,\text{V}^{-1}$$

This also shows, that both parts are so similar in behavior, that a single sides observations would have sufficed.

3.3. 1.8V Regulation

As described beforehand the output voltages for both analog and digital can be adjusted to some degree and therefore we can compensate for the dropoff occurring between PowerIt output terminals and reticles.

The following experiments were run unsing the Power Wafer setup. To run any test with the PowerWafer, the patterns in figure 3.9 were used. There are two reasons for that, firstly these patterns distribute the current draw in a regular fashion as to distribute the load between the connectors. Secondly, when powering Reticles all of the energy is converted into heat, via the ohmic resistors.

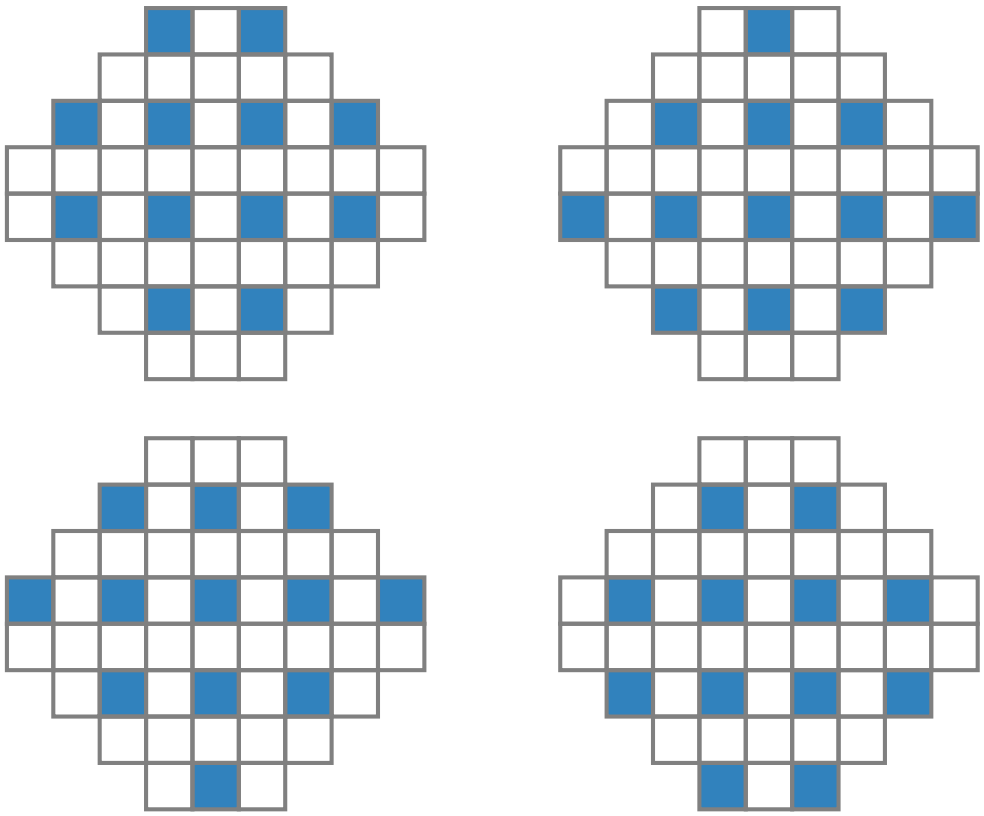

Figure 3.9.: Used regular patterns for current tests on PowerWafer

And although the copper heat sink and fans (see figure 3.2), should be able to handle this heat in a HICANN wafer system, when grouping together reticles and powering them, the thermal conductivity does not suffice. This is the case, because the Power Wafer is drawing more current per reticle than a HICANN wafer would during an experiment. The internal temperature probes (between heat sink and wafer) register well above 50 °C, when grouping 3 or more reticles. The observed overheating can be mitigated using the in figure 3.9 visualized patterns.

3.3.1. Characterization of Dropoff

Wanting to observe and characterize the voltage drop, first the connections between PowerIt and reticles need to be measured with the in figure 2.8 described connections, which in actuality are the PowerIt terminal and corresponding analog readout pin on a AnaB.

To use the Power Wafer, one of the patterns in figure 3.9 will be used, each pattern has a approximate current draw of 120A and will distribute heat and draw per terminal evenly.

In figure 3.10 a single reticles (#40) voltage drop for different current draws is visualized. A relatively linear trend can be observed. While the residuals look like the error could be systematic, with only 12 datapoints that is purely speculative.

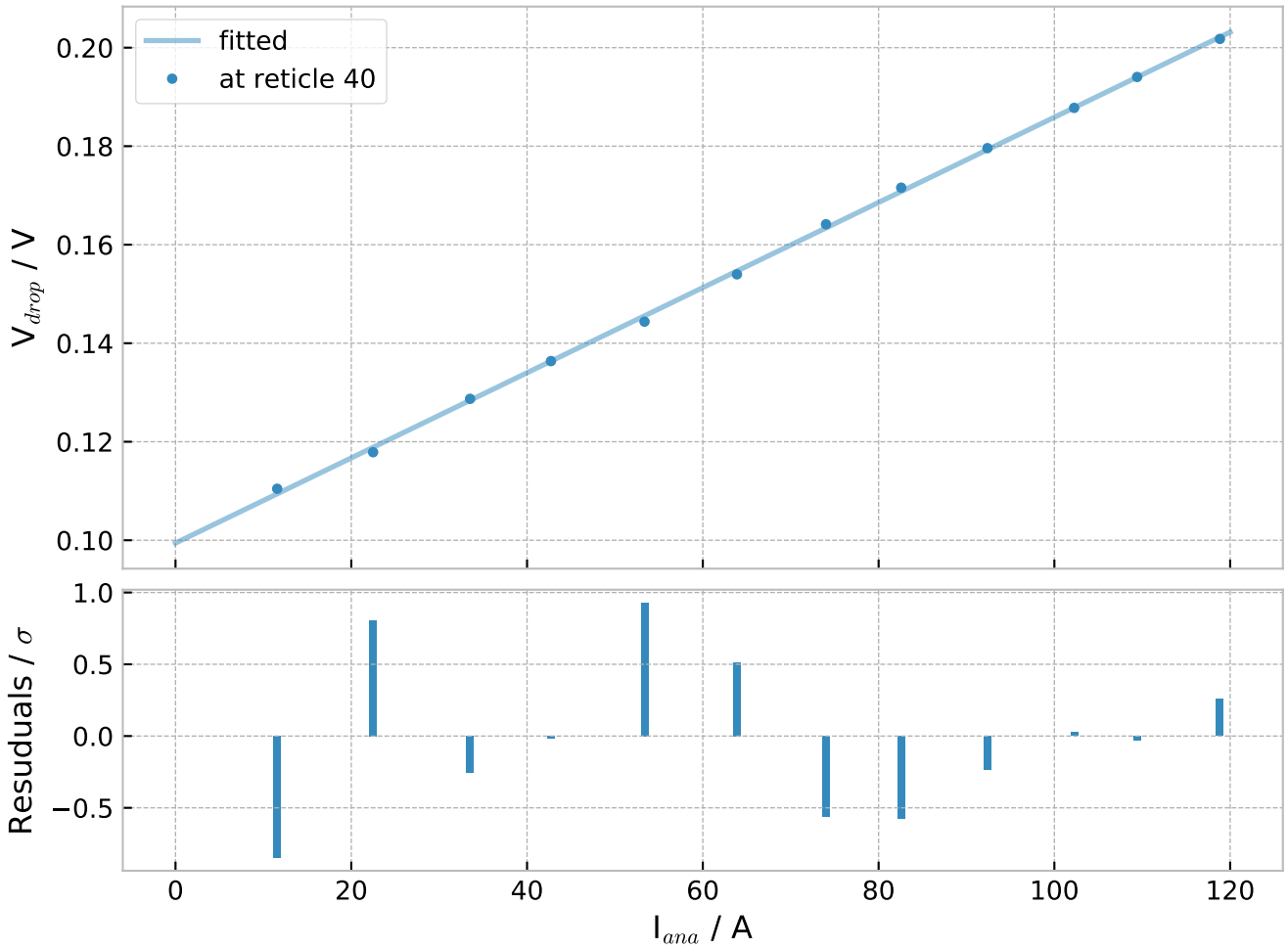

Figure 3.10.: Voltage drop observed between PowerIt and reticle #40, each point represents a state after enabling additional Reticles on the PowerWafer (right upper wafer in figure 3.9)

Here a voltage drop vs. current draw of the wafer shows a linear behavior and therefore can be regulated on basis of the current measurement done by on board measurement circuitry.

3.3.2. Numerical-Correction (Regulation)

The initial idea, to approach the correction of this dropoff is a numerical: the SWRM (subsection 2.2.3) and its corresponding equations can be applied here. Equation 2.16, which maps the measured output current to a corresponding potentiometer setting, requires the dropoff to be linear, which was observed.

To apply this approach, two assumptions need to be made:

- all reticles have the same current draw (already not accurate, see figure 3.10)
- all reticles experience the same voltage drop (as observed for reticle #40)

and the following four values are required, before a regulation can be attempted:

- I_{ret}, the current draw of a single reticle,
- R_0, the resistance between PowerIt and FET,
- R_1, the resistance of the connection between FET and reticle
- V_{off}, the desired voltage at a reticle (users choice)

To get a representative value of I_{ret} for use in the SWRM, the mean current draw per reticle was taken (figure 3.11):

$$I_{\text{ret,mean,corr}} = (9.9 \pm 0.6)\,\text{A} \tag{3.4}$$

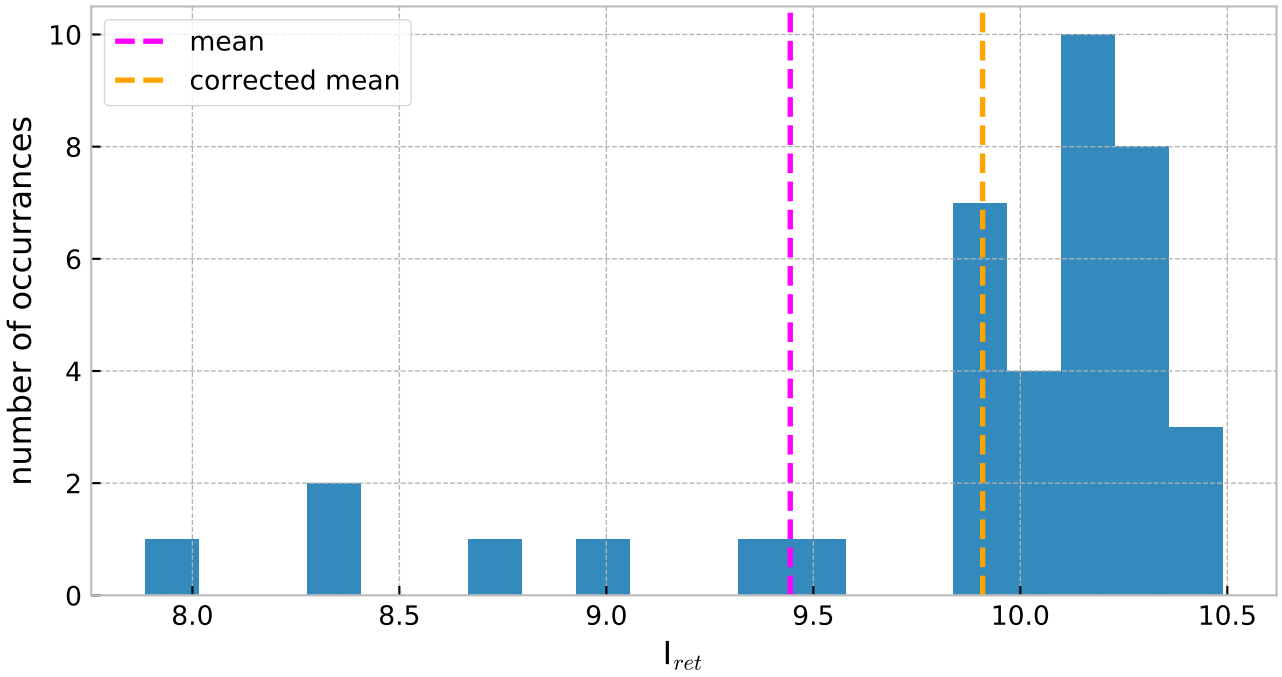

Figure 3.11.: Distribution of analog current draw for all reticles on the PowerWafer (which were possible to measure)

The figure 3.11 was obtained by measuring the increase in current draw for each reticle and each of the 4 patterns (figure 3.9).

To obtain the limits of R_0, the pattern in figure 3.12 was used to take measurements for both the neighborhood as well as the farthest reticles.

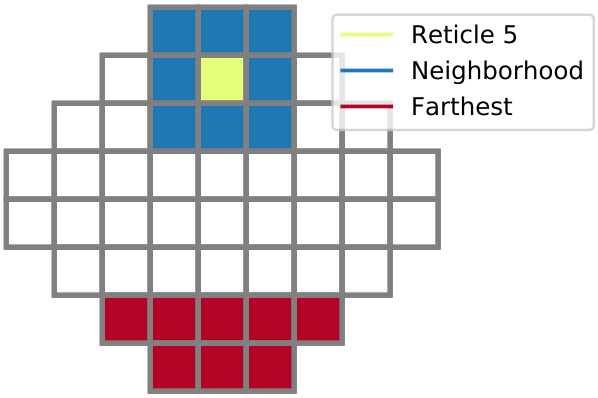

Figure 3.12.: Reticles used to determine correlation between distance and voltage drop

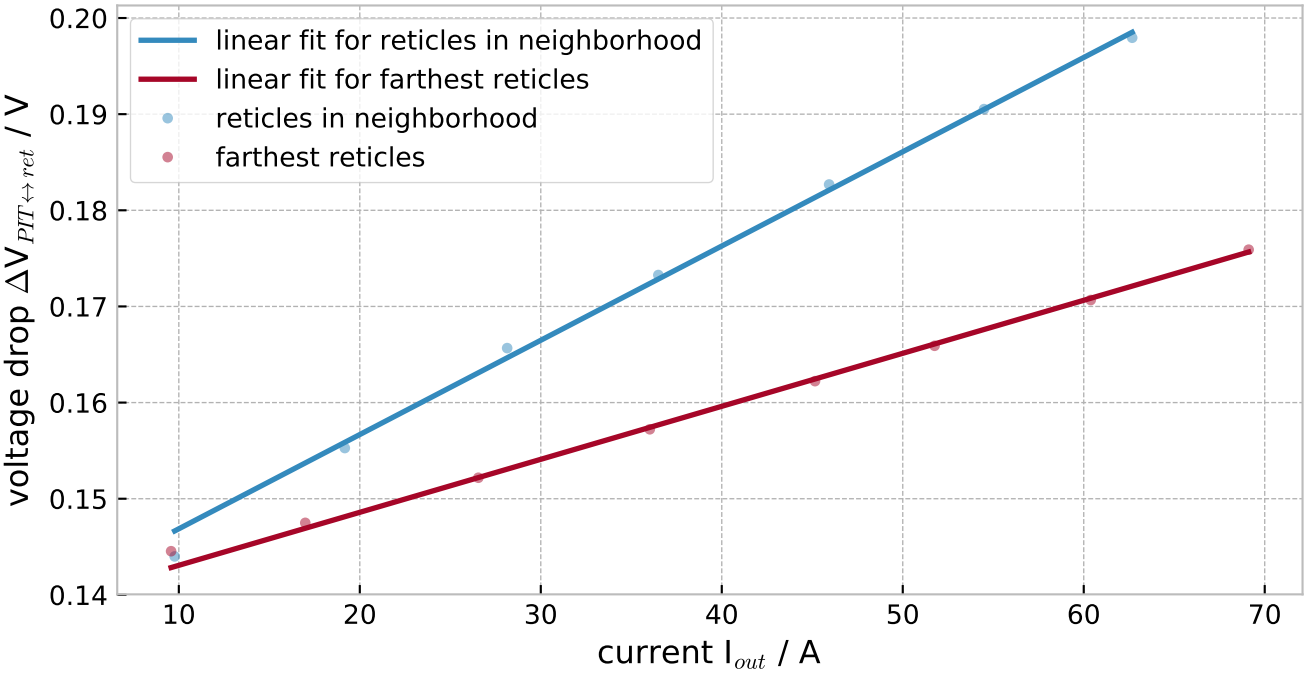

Figure 3.13.: Voltage drop vs current for both reticles in direct neighborhood and farthest possible reticles

From figure 3.13 it is possible to see that the distance between reticles that are used, gives different behavior of the voltage drop. Both inclines happen to be the extreme cases, while either being completely uncorrelated, the case for farthest Reticles, or being directly correlated by their distance, here observable for the neighboring Reticles.

Therefore we obtain two values for R_0:

$$R_{0,\text{neighbor}} = (7.1278 \pm 0.1567)\,\text{m}\Omega$$
$$R_{0,\text{farthest}} = (4.0079 \pm 0.0537)\,\text{m}\Omega \tag{3.5}$$

from the same measurement it is also possible to extract R_1 by extrapolating to 0, which results in:

$$R_{1,\text{neighbor}} = (14.1708 \pm 0.1779)\,\text{m}\Omega$$
$$R_{1,\text{farthest}} = (14.2218 \pm 0.1503)\,\text{m}\Omega \tag{3.6}$$

here the values obtained are within error margin of each other.
So applying these Values, the following behavior for regulation can be visualized.

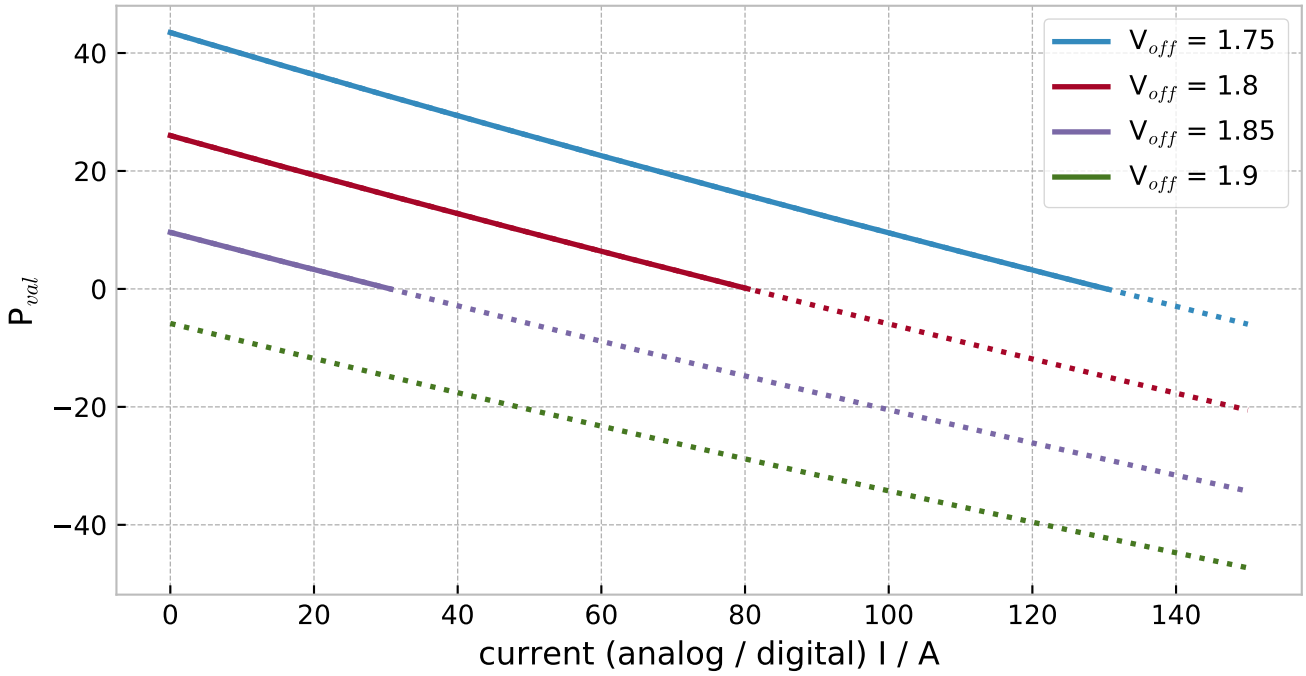

Figure 3.14.: Possible P_{val} curves after SWRM, dotted lines represent not achievable values. This plot is generated from the obtained SWRM parameters, leaving only V_{off} to vary.

The in figure 3.14 visualized values show the theoretical P_{val} for the corresponding current. All of the dotted parts depict with this setup unachieveble values. This results in the PowerIts inability to correct for any change in current above a certain threshold. In the domain above this threshold the resulting voltage would behave the same as before regulation. Note that the 1.8V regulation, should fail at about 80A of current draw.

Now voltage drop per reticle, in a single reticle power state, was observed:

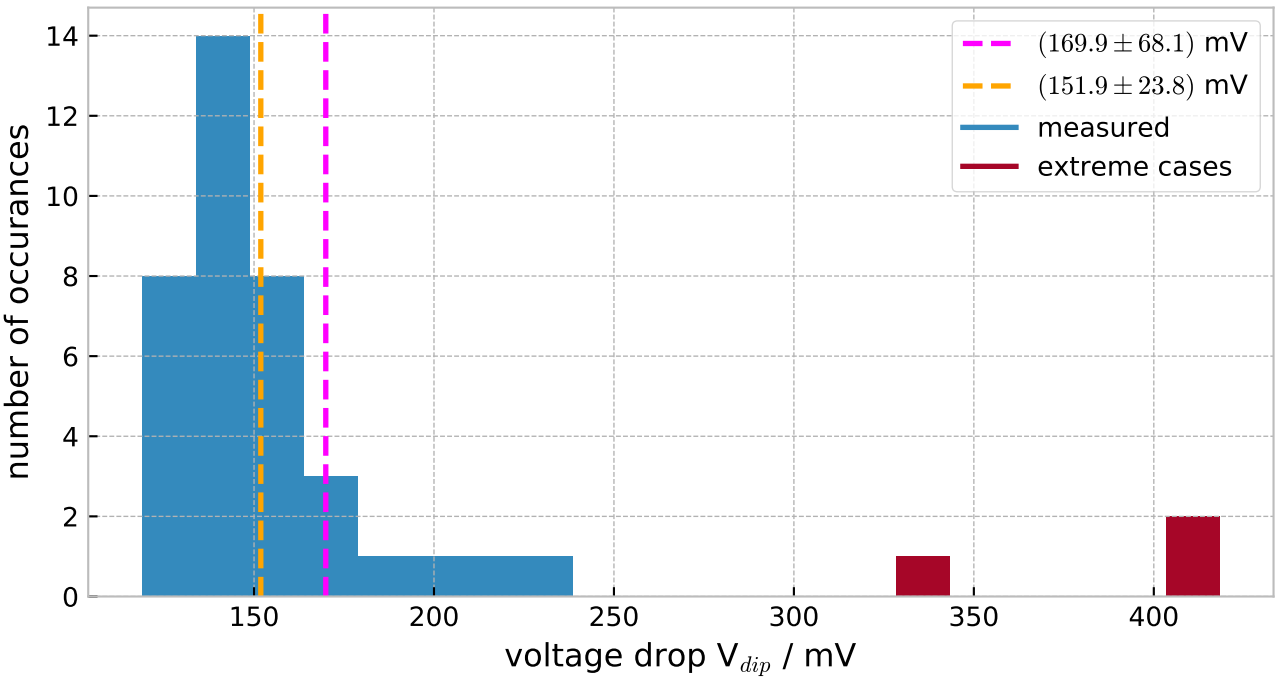

Figure 3.15.: Initially observed voltage drop, red values are ignored for corrected mean

The histogram in figure 3.15 has a corrected mean of

$$V_{\text{dip,mean,corrected}} = (151.8811 \pm 23.8138)\,\text{mV} \tag{3.7}$$

The here obtained mean was taken without the in figure 3.15 as red marked outliers. The reason beind that was that this model should apply for most cases and not include outliers as not to inflate the V_{drop} distribution range.
Figure 3.16 shows how those voltages are distributed over the complete PowerWafer. All white reticles are not measurable, either because they were not functional or could not be read. The occurances marked in red in figure 3.15 are reticles #11, #20 and #28, which were outliers and are excluded in the calculation of corrected values.

This results in a distribution, which when combined with the spread of R_0 from figure 3.13, gives an approximate range for all reticles voltage drop at a given current draw (figure 4.3).

To be able to obtain the through AnaB pins measured voltages it should also be possible to use the CUREs voltage readout. The voltages obtained from these boards, should be comparable. The reason for that is that we can assume a constand R_1 for all reticles. In figure 3.17 these voltages are visualized, in comparison to the AnaB voltages.

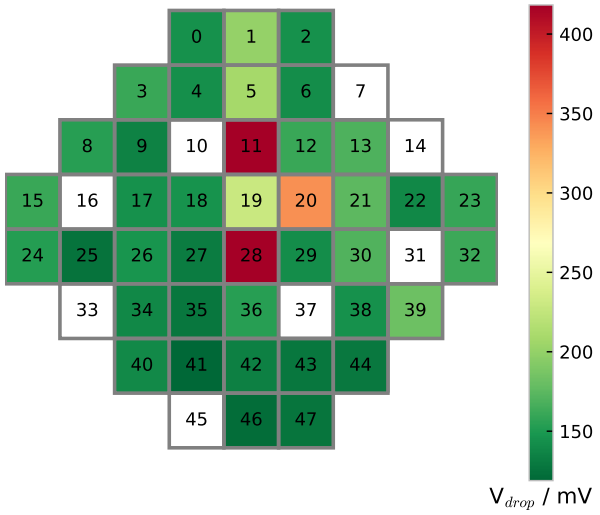

Figure 3.16.: V_{drop} distribution over full Power Wafer; White have no measurement; Red an Orange are marked red in figure 3.15

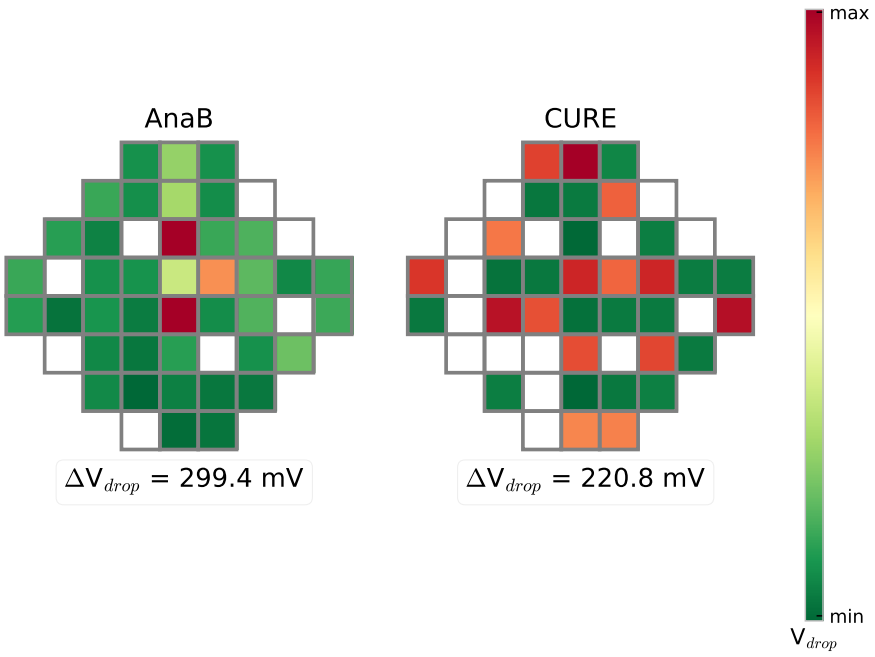

Figure 3.17.: Comparison of AnaB and CURE measured voltage drop. Colors indicate their respective relative values for each measurement. White reticles have no measurement.

This comparison shows no discernable relation between both measurements. The reason for this is most likely a problem in the assumption, that R_1 is the same for all reticles, which would result in a voltage difference that is constant. Additionally the distribution of CURE voltages would look similar to the AnaB measurement.

4 Results

In this chapter all results from the experiments, as well as reasons will be discussed.

4.1. Calibration

This calibration process yielded some workflows for use inside the system as well as calibration values for the used PowerIt.

4.1.1. Calibration-Database

The obtained calibration values for the in these experiments used PowerIt, are combined in code 1.

```
---
id: '0x280029000F51333332343638'
name: B05
poly18iana: [-31.5155, 78.516, -0.0688]
poly18idigi: [-31.3536, 78.3701, -0.196]
poly18i: [-31.4396, 78.443, -0.1324]
poly48i: [-0.1765, 153.0021, -204.1858]
poly10v: [0.6348, 3.459, 0.1118]
poly48v: [-4.5248, 33.3195, -1.6167]
poly18v: [0.0234, 0.9728, 0.0072]
```

Code 1: PITDB entry for B05 PowerIt. `id` is obtained by the firmware and unique to each STM32Chip. The `name` corresponds to the label on each PowerIt. All `poly*` values are all polynomial coefficients in order of 0th degree to 2nd degree.

And to compare, the values in code 2 are theoretical values, obtained from all equations in chapter 2.

```
---
uuid: 'default'
name: 'Bxx'
poly18i: [-3.0, 25.0, 0.0]
poly48i: [0.0, 227.27, 0.0]
poly10v: [0.0, 4.0, 0.0]
poly18v: [0.0, 1.0, 0.0]
poly48v: [0.0, 27.386, 0.0]
```

Code 2: Default PITDB entry for any PowerIt. All `poly*` values are all polynomial coefficients in order of 0th degree to 2nd degree.

4.1.2. Accuracy

To obtain an accuracy for the internal measurements, the experimental sweeps can be repeated after calibration. One example of a calibrated measurement can be seen in figure 4.2.

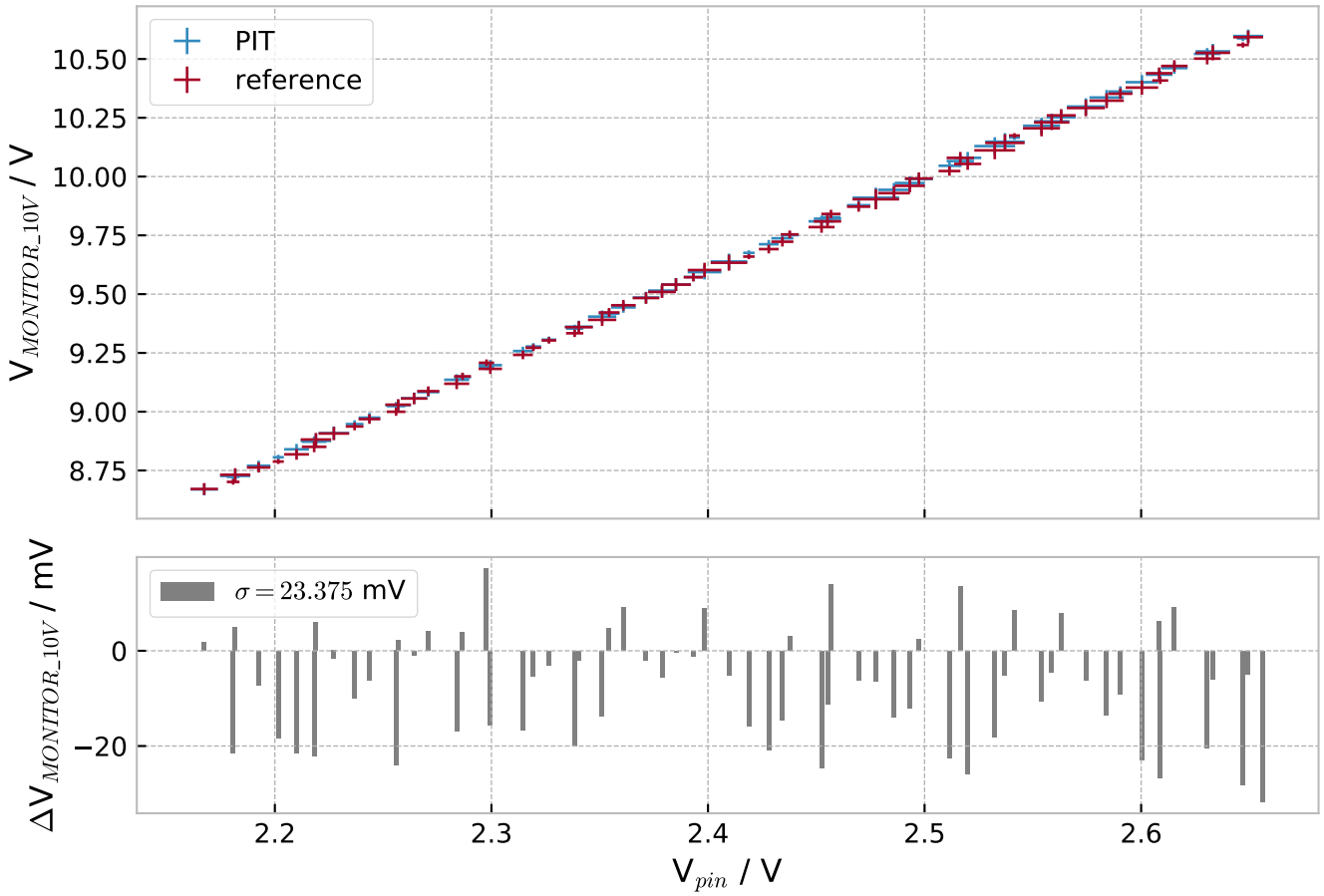

Figure 4.2.: Voltages after calibration. Sweep from 43.2 V to 52.8 V input voltage resulting in a range from 8.64 V to 10.56 V. The errors in the bottom diagram show the differences between reference and PIT values.

This repeats the calibration measurement for 9.6 V. Here quite similar values can be observed, with a maximum ΔV of around 31.7 mV ($\approx 0.33\,\%$). It is also possible to see a systematic error in figure 4.2. This error could be corrected, but requires further iterations of the calibration procedure. Additional iterations would allow for a reduction of ΔV, up to a value of 24.5 mV ($\approx 0.25\,\%$).

In comparison to this, the 1.8 V measurement should have a bit better accuracy because of the even simpler circuit.

$$0.33\,\% \cdot 1.8\,\text{V} \approx 5.9\,\text{mV}$$
$$0.25\,\% \cdot 1.8\,\text{V} \approx 4.5\,\text{mV}$$

And also the accuracy of measuring 48 V should be worse than 24 mV, again because of the circuits complexity.

$$0.33\,\% \cdot 48\,\text{V} \approx 158\,\text{mV}$$
$$0.25\,\% \cdot 48\,\text{V} \approx 120\,\text{mV}$$

4.2. Regulation

These are the obtained results from attempting to regulate the 1.8 V terminals.

4.2.1. Without Regulation

Before the regulation could be attempted some parameters were needed to complete the SWRM, see equations 3.4, 3.5 and 3.6. With these values and their respective (error) ranges the in figure 4.3 found plot could be created.

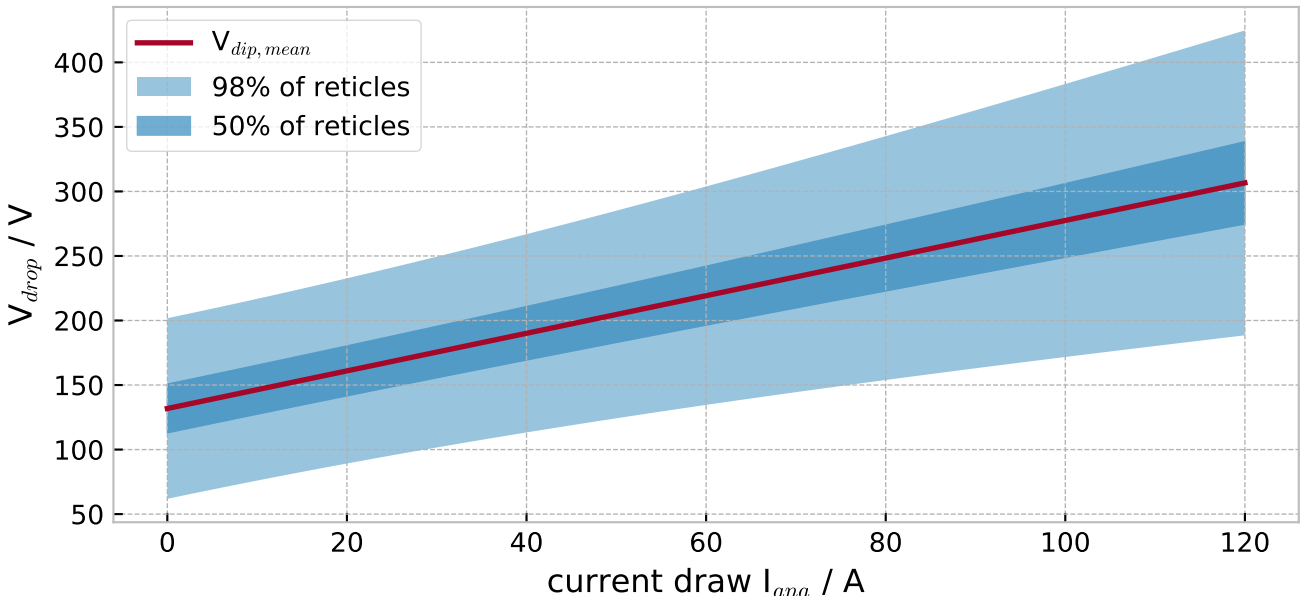

Figure 4.3.: Plot of the expected range of V_{drop} for different current draw. This result is the expected spread without any regulation. Shown are the range for 98% and 50% of reticles, as well as the mean V_{drop} for all reticles.

In figure 4.3 the expected spread of V_{drop} can be found. This spread is the worst case V_{drop} distribution. The reason for that is that with a regulated voltage a constant V_{drop} is expected. This applies to all currents up until $\approx 80\,A$, becase from there the regulation would not work anymore and V_{drop} would behave like in the unregulated case.

4.2.2. With Regulation

To verify the regulation is working and to see if the prediction in figure 3.14 is correct new values were measured. These values are the voltages with regulation enabled at different reticles (see figure 4.4).

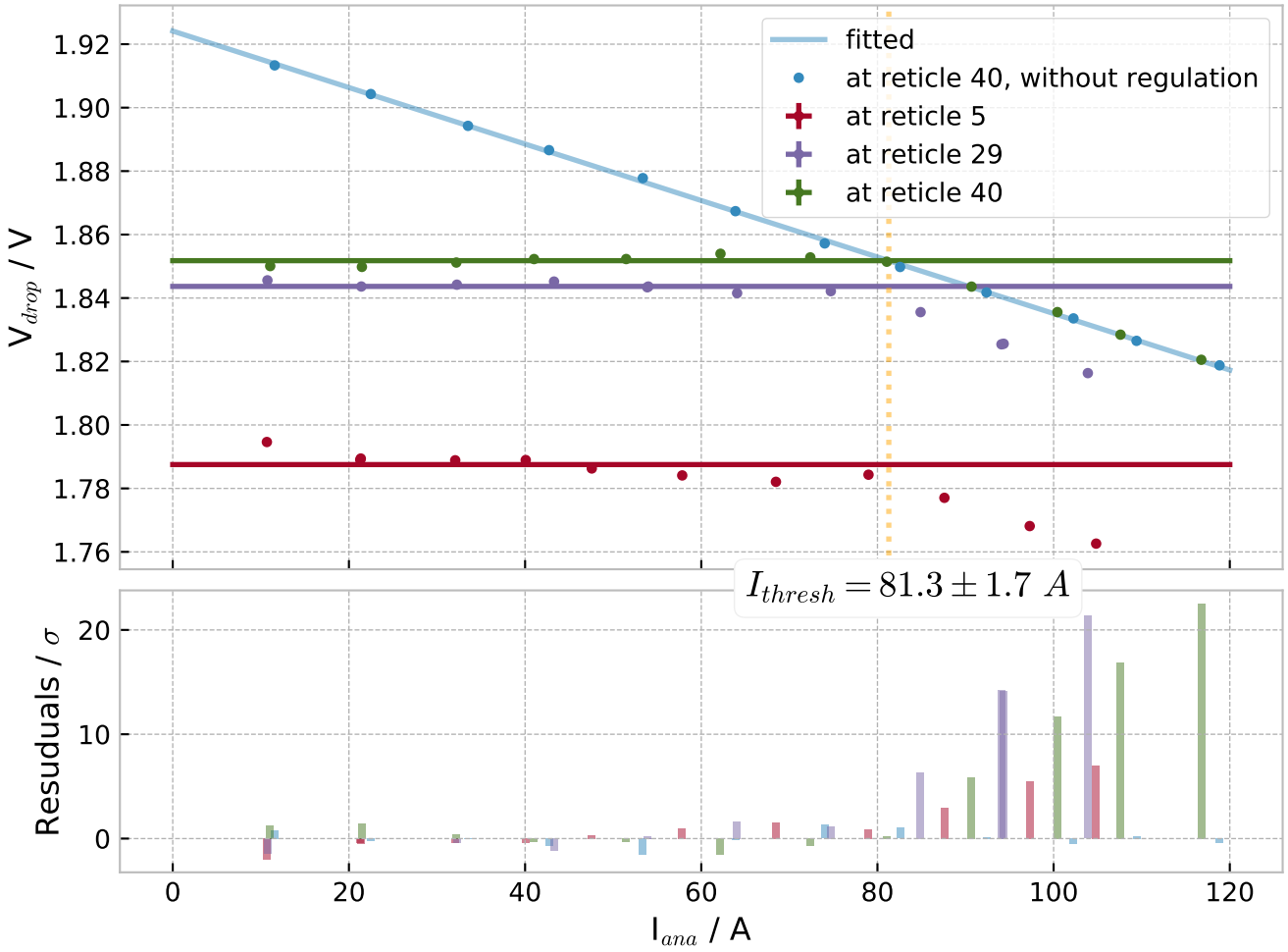

Figure 4.4.: Observed reticle voltages V_{ret} before or after regulation, at multiple reticles. Reticle #40 shows the best-case scenario with the least amount of V_{drop}. Reticle #5 is a worst-case scenario, with the highest V_{drop} while still being placed central.

In figure 4.4 three different reticles (#5, #29 and #40) were measured. Observable is, that firstly the regulation, which was set to achieve 1.8 V is working until I_{ana} is at $I_{thresh} = 81.3$ A. There the minmal potentiometer setting is used. From here V_{drop} behaves the same as without regulation.

Secondly V_{drop} for different reticles is different. This was one of the assumptions in the SWRM. To describe that behavior a distance based model (subsection 4.2.3: DWRM) could be the solution.

The residuals observed are the result of the $I_{ana} > I_{thresh}$ not regulated V_{drop}.

Also, the expected behavior from section 4.2 can be observed.

Additionally if the range of $I_{ana} > I_{thresh}$ is observed, V_{drop} does not increase by more than about 30 mV.

4.2.3. Distance Wafer Resistance Model (DWRM)

So far, the discussed measurements and SWRM have been enough to create a first iteration regulation mechanism. Until now assumptions like a constant R_0 over the complete wafer, have

driven the creation of equations to satisfy this model. They also led to observable inaccuracies, as seen in equation 3.5. Although the SWRM approximates the real world, it is not exact enough. To further develop a model that could describe the real world setup in a better way, the next model would have to describe e.g. a different R_0.

In a wafer, the distance between reticles and voltage connector (see figure 2.7) are resulting in additional resistance.

Therefore the DWRM could be adapted. Circuit 4.5 visualizes a model, in which each different distance from the voltage connector, is classified with an additional resistance.

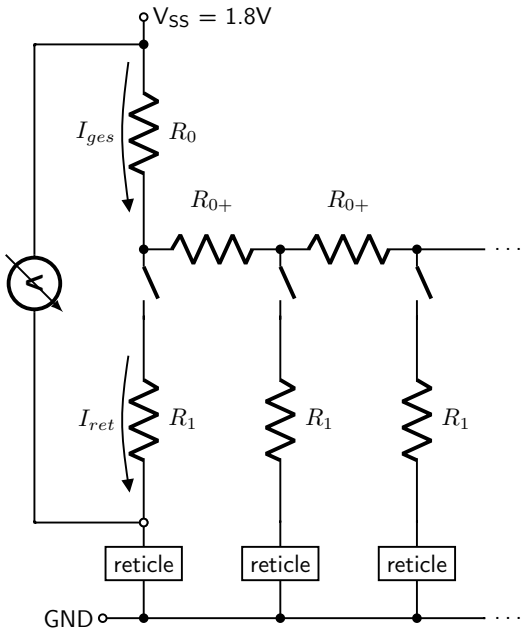

Figure 4.5.: Modified model of the to measure resistances and their currents. Similar to SWRM R_0 describes the resistance of the shortest connection between the PowerIt output, up to the FET (depicted as switch), while R_1 is a resistance between FET and reticles. But additionally R_{0+} described a resistance, that depends on the distance between reticle and voltage connector. The measurement is done between output terminals on the PowerIt and pins on a AnaB.

With this model the voltage is now expected to change depending on the reticles distance instead of being the same. The distances inside a wafer are visualized in figure 4.6

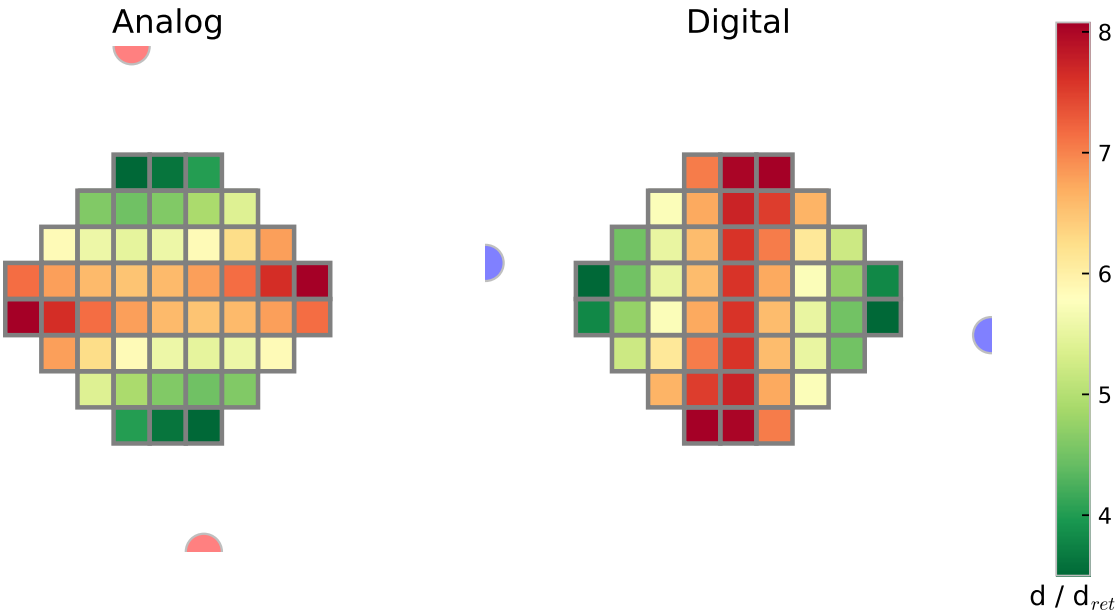

Figure 4.6.: Distances of reticles to the nearest voltage supplying connection for DWRM, distance is normed to the reticle-side length

5 Outlook

While all of the measurements could be calibrated they can still be fine tuned. The found accuracy was $\approx 0.33\,\%$. To gain a better accuracy would require further iterations of the calibration process. In the future it should also be possible to make these even more accurate, either by using a different method than the internally used polynomial of second degree. This calculation could be of third degree or not even a polynomial.

The voltage distribution over the complete wafer was measured. Using this distribution and V_{drop}s behavior at different loads could then be combined with the first iteration regulation model (SWRM). This produced both the worst-case V_{drop} range as well as a set of formulas which could be used further. These formulas allowed for regulating the 1.8 V terminals. Additionally a threshold current I_{thresh} could be observed. This current limits the regulation mechanism, and results in still usable, but unregulated V_{drop}. This threshold current was also predictable with the theoretical considerations. To further develop this mechanism, another, more complex, model (DWRM) was proposed. The DWRM would allow for a more accurate regulation, which is specific to a given experiment and its chosen reticles. This model would narrow down the worst-case scenario depicted by figures 4.3 and 4.4. For that model to work, each experiment run on a HICANN wafer, would require a simulation of the distribution of voltage between the used reticles. This would minimize the maximum difference in voltage drop considerably.

Furthermore the observed current threshold of 81.3 A is restricted by a internally used resistor value. If the minimum resistance of the 1.8 V generating circuit were to be decreased, the threshold would increase.

There are also external effects wich were not covered in this thesis. One of those is that all systems are subject to temperature changes and therefore might not be stable or noisy. Investigating this dependency would also allow for possible regulation mechanisms to compensate for changes in temperature.

Running a calibrated and regulating PowerIt inside a HICANN wafer system, would be the next step in testing the regulation mechanism. The now regulated voltages could be resulting in more stable experiments. It would also be feasable to now test the influence of different voltages on the wafers neuromorphic chips and their calculations. Additionally to run an experiment on a HICANN wafer, a calibration is needed, and could also be influenced by the now regulated 1.8 V voltages.

I Appendix - Firmware

I.1. Virtual Memory Mapping

The biggest change done to the firmware was the implementation of a new communication protocol.

addr	name	type	size	perm
0x00	onmask	byte	1	rw
0x01	offmask	byte	1	rw
0x02	anapot	9bit	2	rw
0x04	digipot	9bit	2	rw
0x06	polyFit.V48	float arr	12	rw
0x12	polyFit.I48	float arr	12	rw
0x1e	polyFit.V8	float arr	12	rw
0x2a	polyFit.V18	float arr	12	rw
0x36	polyFit.I18	float arr	12	rw
0x42	polyFit.T	float arr	12	rw
0x4e	sampleTicks	byte	1	rw
0x4f	V_out	float	4	rw
0x53	TEMP_SENSOR	float	4	r
0x57	EXT_AIN	float	4	r
0x5b	MONITOR_48V	float	4	r
0x5f	MONITOR_48I	float	4	r
0x63	MONITOR_8VBUS	float	4	r
0x67	MONITOR_8IBUS	float	4	r
0x6b	MONITOR_8V_0	float	4	r
0x6f	MONITOR_8V_1	float	4	r
0x73	MONITOR_8V_2	float	4	r
0x77	MONITOR_8V_3	float	4	r
0x7b	VDD_1V8_ANA	float	4	r
0x7f	VDD_1V8_IOUT_ANA	float	4	r
0x83	VDD_1V8_DIGI	float	4	r
0x87	VDD_1V8_IOUT_DIGI	float	4	r
0x8b	CommitHash	float	4	s
0x8f	CommitDirtyFlag	byte	1	s
0x90	STM32UUID	96bit	12	s

Figure I.1.: memory mapping of the packed struct moved over i2c, `addr` is the address to use, `type` is the c++ type, `size` is in bytes and `perm` denotes read-writability. writability

This protocol uses the table from figure I.1 as reference.

I.2. How to calibrate a PowerIt Board

The calibration process is based on the PItSTOP python scripts. These are split into `server` and `aggregator`. While the server is handling the translation between raw I^2C data, and the JSON formatted result, the aggregator takes this JSON and calculates a calibration.

Using the script any one of the following values can be tested and calibrated:

- input voltage (`pitstop.Aggregator.test_v_48()`)
- input current (`pitstop.Aggregator.test_i_48()`)
- 9.6V output voltage (`pitstop.Aggregator.test_v_10()`)
- 1.8V output voltage (`pitstop.Aggregator.test_v_18()`)
- 1.8V output current (`pitstop.Aggregator.test_i_18()`)

I.2.1. Setting up the Test Environment

The simplest way to setup an environment consists of cloning the PItSTOP project on a client:

```
> git clone ssh://git@gitviz.kip.uni-heidelberg.de/sw-stm32.git
```

then substituting the `rsync` target:

```
all:
    rsync --progress ./*.py /remote.url/
```

, to be your server (should be a RaspberryPi connected to the PowerIt)

I.2.2. Running a Test

Running the test requires the following commands
serverside:

```
> python server.py
```

clientside:

```
> python aggregator.py
```

Now just following the instructions given, the selected test can be run:

```
Setting up calibration test for {}
Please be sure to:
 - connect the {} to the RaspberryPi running server.py.
 - connect the PowerIt to the RaspberryPi as described in the
  ↪  documentation
 - and be sure to connect the {} to the {} Terminal.

Continue (y/N): y

What is the Name given to the connected PowerIt? [Bxx]: B05
```

The result will consist of two diagrams one without calibration and one with. It will also write the newly obtained calibration data into `pitdb.yaml`

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Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, 29. August 2018,

.....
(signature)