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Bachelor Thesis in Physics
submitted by

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Calibration of BrainScaleS PowerIt Subsystem and Regulating a BrainScaleS Power Supply

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Abstract

Accurate measurements and voltage supply is a integral part for any system to work perfectly. In the Human Brain Project framework this thesis will provide a calibration of the BrainScaleS PowerIt Subsystem as well as a regulation mechanism for a BrainScales power supply.

It will give insight into the internal workings of the PowerIt. Its circuitry will be examined and calibrated, for use in BrainScaleS' monitoring. And a method for regulating one of its power Supplies will be implemented, based on observations done with an experimental setup of a in BrainScales deployed Wafer System.

This thesis also contains the changes done to the PowerIt Firmware while working on these Problems. The main focus layed on a new interfacing protocol. It can now be used for accessing the calibration and regulation parameters as well as their respective measured values .

Zusammenfassung

Das akkurate messen von und versorgen mit Spannungen ist ein integraler Teil jedweden elektrischen Systems, sodass diese reibungslos funktioniert. Innerhalb des Bereiches des Human Brain Projektes, liefert diese Arbeit die Kalibration des BrainScaleS Teilsystems PowerIt, sowie die Regulierung einer Spannungsversorgung des BrainScaleS.

Diese Arbeit verschafft einen Einblick in den internen Aufbauu des PowerIt, dabei werden dessen Schaltungen untersucht und kalibriert, sodass diese in der Systemüberwachung nutzbar sind. Ausserdem lifert diese Arbeit eine Methode der Regulation für eine der Sapnnungsversorgungen. Diese basiert vor allem aif den Beobachtungen mittels eines experimentellen aufbaus eines in BrainScaleS genutzten Wafer Systems.

Zusätzlich enthalten sind die Änderungen, die an der PowerIt Firmware vorgenommen worden sind. Dabei liegt der Fakus auf einem neuen Protokoll zur kommunikation, welches dafür genutzt werden kann die Parameter und Werte der Kalibration und Regulation auszulesen oder zu setzen.

Contents

1 Introduction

1.1. The BrainScale System

The BrainScale Wafer System, developed and used in the electronic visions group at Heidelberg University is a neuromorphic hardware implementation [1].

For this thesis the following core components are of importance:

- mixed-signal ASICs, named HICANNs, structured in packs of 8 into reticles
- Control Units for Reticles, short CURE boards
- Analog Breakout boards, AnaB for short
- and power supply, called PowerIt.

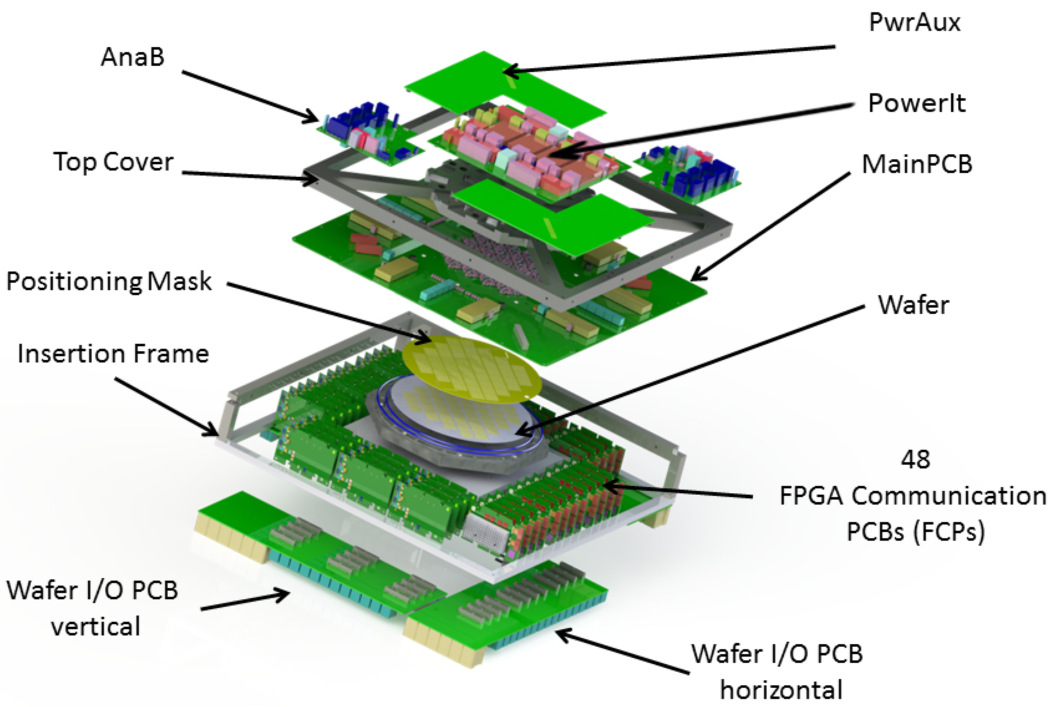

Figure 1.1.: The BrainScaleS wafer-scale hardware system, marked are the main components comprising a single wafer system. [2]

1.2. About the PowerIt Subsystem

The main subject of this thesis is the PowerIt board (Figure 1.2). It functions as power supply inside of the WaferScale system (Figure 1.1). In which it is providing the wafer with 1.8 V and the FPGAs with 9.6 V. Its maximum rated power draw is 2 kW. [3]

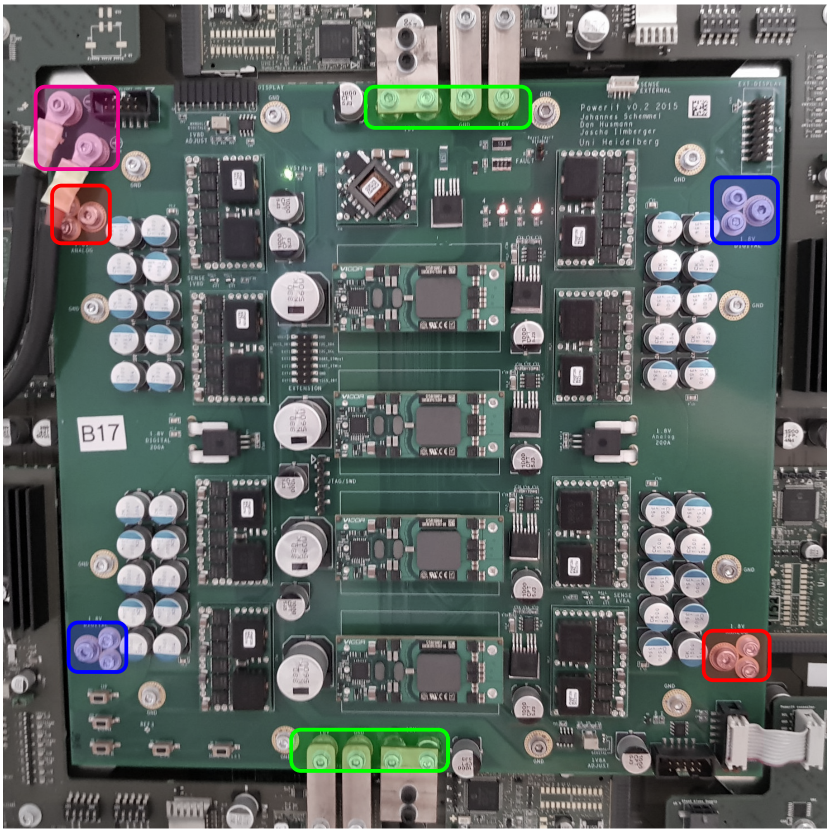

Figure 1.2.: PowerIt board, top view, receiving 48 V as input (magenta) and outputting 9.6 V (green) as well as 1.8 V (analog: red, digital: blue)

The brain of these PowerIt boards is a STM32 Chip[1] which runs a custom firmware based on ChibiOS [5]. The PowerIt, while providing 9.6 V and 1.8 V, also is able to measure the following values:

- input voltage and current
- 1.8 V output voltage and current
- and the 9.6 V output Voltage

which can then be used inside the firmware.

While the input voltage is given from outside it is still changeable if the power supply is able to vary its output voltage. Additionally the 9.6 V are a set voltage obtained by the power supply modules[2], which divide the input volatge by 5. Lastly the 1.8 V output voltage is variable.

[1]STM32F405RGT [4]
[2]5:1 Bus converter IB0xxE096T48xx, 500W each

1.3. Contents in Detail

The first goal was to be able to change the calibration parameters. While this can be done at compile time, these changes are board specific. Therefore they either need to be changed, before compiling, which would require a compilation per board. Or else the need to be able to change during runtime. For mainly maintainability reasons the second way was choosen.

But these calibration changes could not be transferred to the PowerIt using the old communication protocol, referred to as PItCOMM version 1. A updated protocol was needed and it had to be able to accept not only the before mentioned values, but also any additional information or configuration.

And while at it, the protocol, now PItCOMM version 2, was made to be somewhat compliant with the SMBus specifications. This was accomplished with a virtual memory map, which maps every parameter to a specific location in a virtual memeory. In this memory, any value which needed to be accessible, be it measurement, calibration or static board information, is mapped (see Figure I.2).

With this as foundation, the PowerIt could be calibrated. The parameters obtained by the calibration proces were be stored in a database. The Calibration characterizes the voltage measuring circuit, whose voltages are either coming into or leaving the PowerIt. The same thing applies to the input and the 9.6 V current measuring circuit.

Taking these calibrations as bais, the 1.8 V power supplys' behavior could be observed. Additionally the electrical behavior of actual hardware both static (no currents) and dynamic (changing currents) could be observed. And with these measurements a model was applied and checked for fitting this situation.

Lastly some statements could be made about the complete hardwares bahavior and a first version of a regulation model could be implemented.

2 Theory

This chapter will be discussing the fundamental principles used in the experiments. These will contain simplified circuits and their respective equations as well as component behavior as specified in their respective datasheets by their manufacturer

2.1. Hardware Component Behavior

Before discussing the experimental results it needs to be clear what circuitry is used in these experiments and what behavior we expect. Keeping in mind, that these are theoretical values and will most likely not be exactly the same as those found in actual hardware, as all values given will always be within some error.

Each of the three voltage regimes that will be observed on the PowerIt board, 48 V, 9.6 V and 1.8 V, has a voltage- and in the cases of 48 V and 1.8 V also a current-measurement circuit. Additionally there is a temperature sensor built into the STM32 chip.

2.1.1. ADC Calibration

The measurements will be done by the STM32-Chip, which uses 12bit ADCs. A single ADC will be switching between all connected pins. This Behavior can be problematic in regards to measuring accurately. The timing used to measure a single pin can be programmatically set from 3 up to 480 clock ticks[1]

2.1.2. 48V Input Voltage

The circuits for measuring input voltage and current are the most complex. For voltage measurement the circuit needs to

- divide our input voltage into a usable potential range
- decouple the input (48 V) from signal potential (3.3 V)
- and amplify the voltage, to be in the STM32-Chips Voltage range of up to 3.3 V.

The already implemented cicuit can be seen in Figure 2.1.

It consists of a 1:240 voltage divider, a full differential isolation amplifier taking in the roughly 200 mV (nominal voltage range), and amplifying it by a factor of 8 ($r_{\mathrm{diffOpAmp}}$ [6]). It is also decoupling the input and output voltages, so our 48 V and 3.3 V circuit parts are electrically

[1] this clock is the internal adc clock, with a frequency of 159 Hz

insulated. The remaining operational amplifier provides difference to single ended conversion with an amplification or 1.1 (r_{OpAmp})

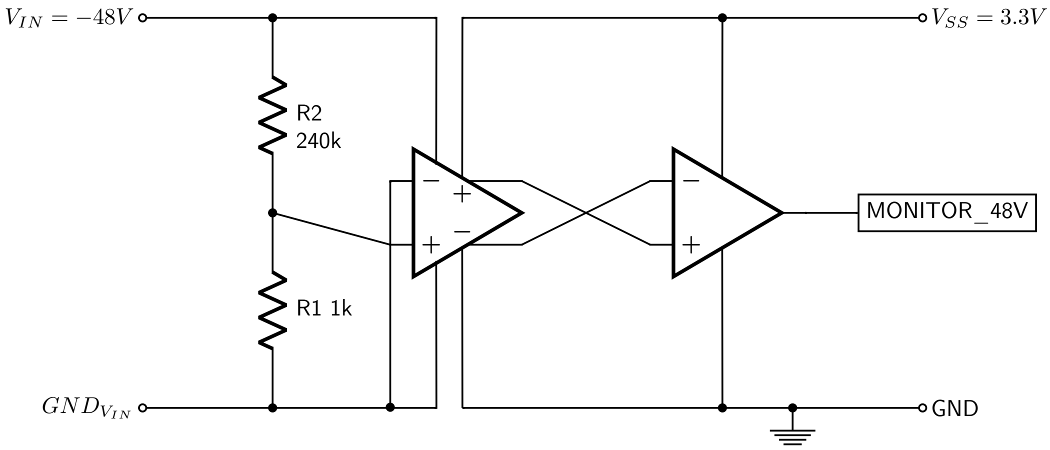

Figure 2.1.: Circuit for measuring the 48 V input voltage, consisting of input potential (left), two resistors as voltage divider, one fully differential isolation amplifier (left), one operational Amplifier (right), output voltage as well as the connection to the STM32-Chips input pin (right)

This circuit results in the following equation for calculating the input voltage from a pin voltage:

$$
\begin{aligned}
V_{\text{48V in}} \cdot \frac{R_1}{R_1 + R_2} \cdot r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}} &= V_{\text{MONITOR\_48V}} \\
\Leftrightarrow \quad \frac{V_{\text{MONITOR\_48V}}}{r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}}} \cdot \frac{R_1 + R_2}{R_1} &= V_{\text{48V in}}
\end{aligned} \tag{2.1}
$$

and the extremes, when assuming $(48.0 \pm 4.8)\,\mathrm{V}$ are

$$V_{\text{MONITOR\_48V, min}} = 43.2\,\mathrm{V} \cdot \frac{1}{240+1} \cdot 8 \cdot 1.1 = 1.5774\,\mathrm{V} \tag{2.2}$$

$$V_{\text{MONITOR\_48V, max}} = 52.8\,\mathrm{V} \cdot \frac{1}{240+1} \cdot 8 \cdot 1.1 = 1.9280\,\mathrm{V} \tag{2.3}$$

2.1.3. 48 V Input Current

The circuit has to satisfy the following constraints:

- use a shunt resistor, with minimal heat dissipation
- while still providing a good resolution within the STM32-Chips specifications

To accomplish that, the circuit is measuring the voltage over a $500\,\mu\Omega$ shunt Resistor, while a current is flowing. By Ohms Law that results in a linear proportionality between current an the obtained voltage. Which is then decoupled and amplified by a factor of 8, as well as converted from a difference to single ended voltage, with a amplification factor of 1.1.

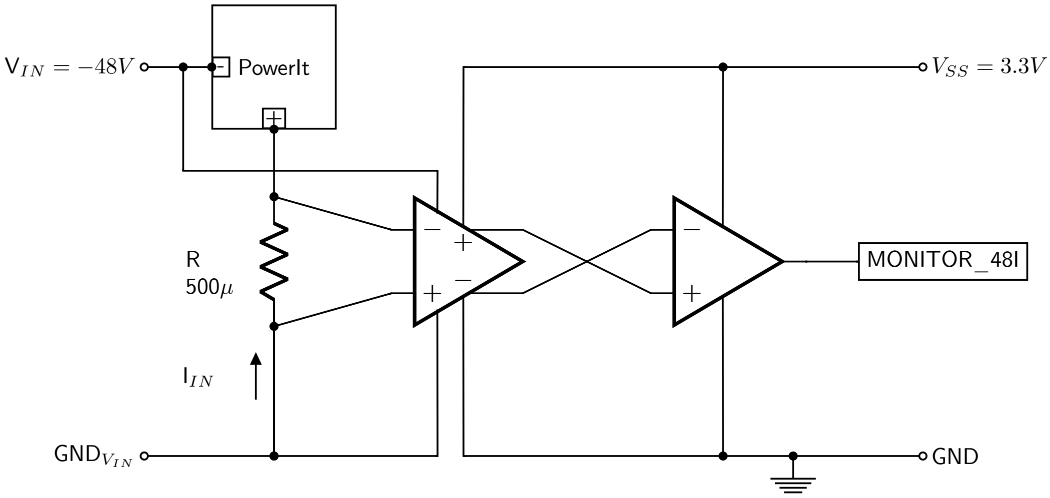

Figure 2.2.: Circuit for measuring the 48 V input current, consisting of the powerit Input circuit, one shunt-resistor, one full diff isolating Amplifier, one operational amplifier, output potential, as well as the connection to the STM32-Chips input pin

Here the same amplifiers as in subsection 2.1.2 is used and so we can apply the following equation for our input current:

$$
\begin{aligned}
I_{\text{48V IN}} \cdot R_{\text{shunt}} \cdot r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}} &= V_{\text{48I pin}} \\
\Leftrightarrow \quad \frac{V_{\text{48I pin}}}{R_{\text{shunt}}} \cdot \frac{1}{r_{\text{diffOpAmp}} \cdot r_{\text{OpAmp}}} &= I_{\text{48V IN}}
\end{aligned} \tag{2.4}
$$

The current range is from 0 A up to 41.7 A (= 2 kW / 48 V)and gives a resulting observable voltage range from 0 V to:

$$
41.7\,\text{A} \cdot 500\,\mu\Omega \cdot 8 \cdot 1.1 = 0.1833\,\text{V} \tag{2.5}
$$

2.1.4. 9.6V Output Voltage

The measurement of 9.6 V is quite simpler. This Circuit consists of a 1:3 Voltage Divider.

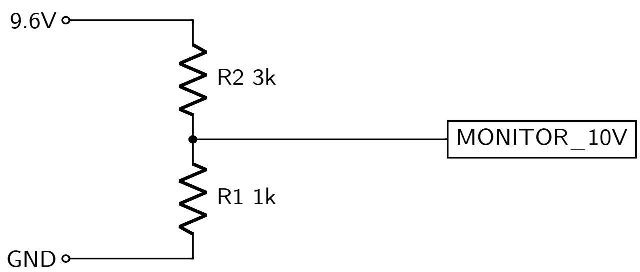

Figure 2.3.: Circuit for measuring 9.6V output voltage. Consisting of a voltage divider with 1:4 ratio, input voltage (left) and output voltage (right)

To describe that circuit the following equation can be used:

$$\frac{V_{\text{9.6V IN}} \cdot R_1}{R_1 + R_2} = V_{\text{MONITOR\_10V}} \tag{2.6}$$

$$\Leftrightarrow \frac{V_{\text{MONITOR\_10V}}}{R_1} \cdot (R_1 + R_2) = V_{\text{9.6V IN}} \tag{2.7}$$

2.1.5. 1.8V Output Voltage

To measure this Voltage the output is directly connected to a pin on the STM32-Chip.

But until now the voltages and current could only be measured, now the mechanism for setting a resulting voltage at the 1.8 V terminals is known. The circuit for generating 1.8 V can be seen inFigure 2.4. It consists of a power module and a resulting resistance between two pins, defined by R_{series}, $R_{parallel}$ and R_{pot}. The resistances job is to set the output to a given voltage of around 1.8 V. That voltage can be varied based on R_{pot}, because this resistance is set via a digital potentiometer[2].

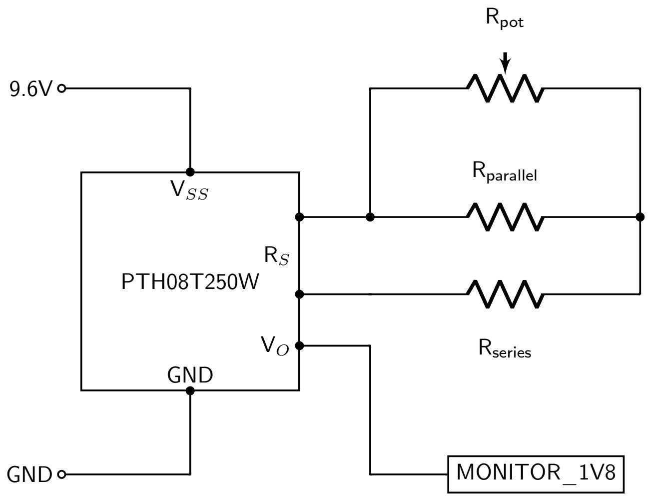

Figure 2.4.: 1.8V supply circuit, featuring a DC-DC Converter, a resistor chain, supply voltage (left) and resulting voltage (right)

The in Figure 2.4 used 1.8 V converter has a characteristic formula [8], and the in this circuit used potentiometer is a linear 10 kΩ Reheostat.

Therefore equations 2.8, 2.9 and 2.10 can describe the circuit.

$$R_{\text{potentiometer}} = P_{\text{val}} \frac{10\,\text{k}\Omega}{256} \tag{2.8}$$

$$R_{\text{SET}} = \left(\frac{1}{R_{\text{potentiometer}}} + \frac{1}{R_{\text{parallel}}} \right)^{-1} + R_{\text{series}}$$

$$= \frac{R_{\text{potentiometer}} \cdot R_{\text{parallel}}}{R_{\text{potentiometer}} + R_{\text{parallel}}} + R_{\text{series}} \tag{2.9}$$

$$V_{\text{MONITOR\_1V8}} = \frac{30.1\,\text{k}\Omega}{R_{\text{SET}} + 6.49\,\text{k}\Omega} \cdot 0.7\,\text{V} + 0.7\,\text{V} \tag{2.10}$$

[2]MCP4152 digital Rheostat [7]

Visualizing the Equation 2.9 results in Figure 2.4, in which the limits of this circuit are visible.

$$V_{\text{MONITOR\_1V8, min}} = 1.549\,\text{V} \tag{2.11}$$

$$V_{\text{MONITOR\_1V8, max}} = 2.022\,\text{V} \tag{2.12}$$

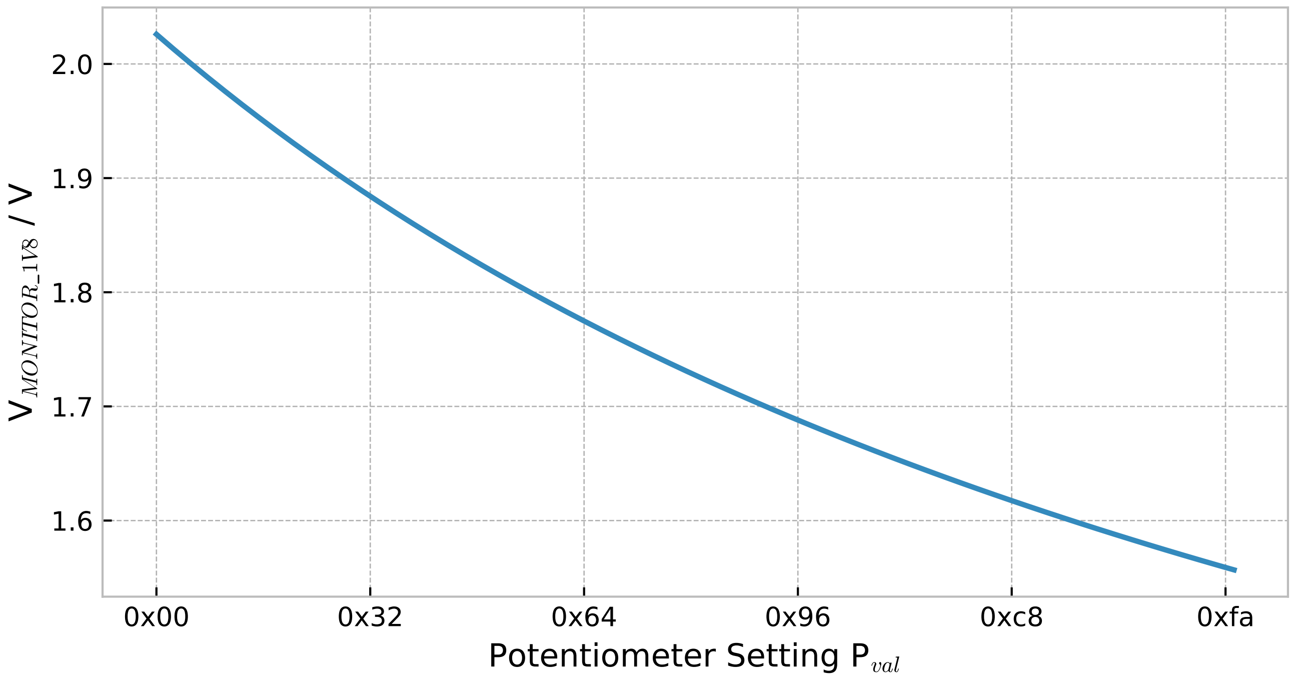

Figure 2.5.: Expected behavior of 1.8V output voltage vs potentiometer setting

2.1.6. 1.8V Output Current

The circuit for measuring the outgoing current over 1.8V, consists of a current sensing IC, which is Hall sensor based. Each connection (digital and analog) has this IC in series to its load.

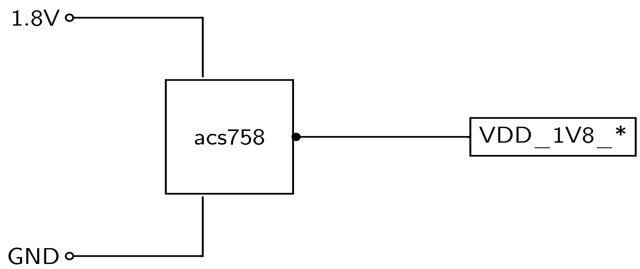

Figure 2.6.: 1.8V current sensing circuit, featuring a acs758, hall sensor based current sensing IC, input voltage (left) and output voltage (right)

The IC is rated for a maximum constant current draw of 100A, and features the following behavior:

$$I_{\text{1.8V, in}} \cdot 0.004\,\text{V}\,\text{A}^{-1} + 0.12\,\text{V} = V_{\text{MONITOR\_1l8}} \tag{2.13}$$

By applying the limits of 0 A and 100 A, the following voltage range can be observed:

$$0\,\mathrm{A} \cdot 0.004\,\mathrm{V\,A^{-1}} + 0.12\,\mathrm{V} = 0.12\,\mathrm{V} \tag{2.14}$$

$$100\,\mathrm{A} \cdot 0.004\,\mathrm{V\,A^{-1}} + 0.12\,\mathrm{V} = 0.52\,\mathrm{V} \tag{2.15}$$

2.2. 1.8V Output Regulation

The method for regulating the 1.8 V output voltage consists of two parts.

First the voltage, wanted at the output terminal and second the corresponding potentiometer setting to use for that voltage On the other hand, to calculate the voltage to output, it is necessary to classify the connections between the PowerIts output terminals and reticles.

2.2.1. Potentiometer Mapping

Combining Equations 2.8, 2.9, and 2.10, we gather Equation 2.16. This equation maps a given output voltage to a corresponding Potentiometer Setting (reverse to Figure 2.5).

$$P_{\text{val}} = \frac{R_{\text{par}}\left[\left(\frac{0.7V \cdot 30.1k\Omega}{V_O - 0.7V} - 6.49k\Omega\right) - R_{\text{ser}}\right]}{R_{\text{par}} + \left(\frac{0.7V \cdot 30.1k\Omega}{V_O - 0.7V} - 6.49k\Omega\right) - R_{\text{ser}}} \cdot \frac{256}{10k\Omega} \tag{2.16}$$

This mapping will be converted into a lookup table before the PowerIt firmware is initiated.

2.2.2. Power Wafer

To test the 1.8 V regulation the so called PowerWafer is going to be used. It can be controlled similar to a in BrainScaleS used, functional, Wafer module. But it is fundamentally different, as it cannot be used for any neuromorphic computations, but only to test for voltages and currents. Its internals are ohmic resistors, which provide a maximum power draw per reticle of what is possible inside a usable wafer module.

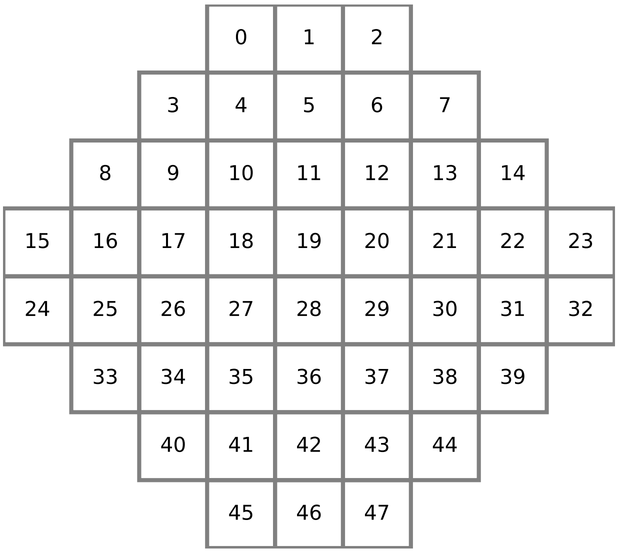

Figure 2.7.: Reticle diagram of a wafer in BrainScaleS. All 48 Reticles are shown. This Layout is an approximation of realworld positioning. A single reticle has a width of 20.0482 mm and height of 20.145 mm, with additional space in between reticles of 420 µm horizontally and 250 µm vertically [1]

It has the same layout as its system counterparts and each of the 48 reticles can be accessed, digitally as well as electrically.

And like its system counterparts it is placed on a MainPCB (see Figure 2.8). All CURE boards connect to it and control the PowerFETs, as well as provide voltage readout from each reticle. The CURE boards read right before R_1 in Figure 2.9.

Also on the MainPCB are the AnaB boards. Note that here lies another specialization of the PowerWafer. All reticles' analog and digital 1.8 V lines are connected directly to pins on the analog readout boards [9]. There it is possible to aaccess a voltage, which is measured after the load resistors in Figure 2.9 (after [1])

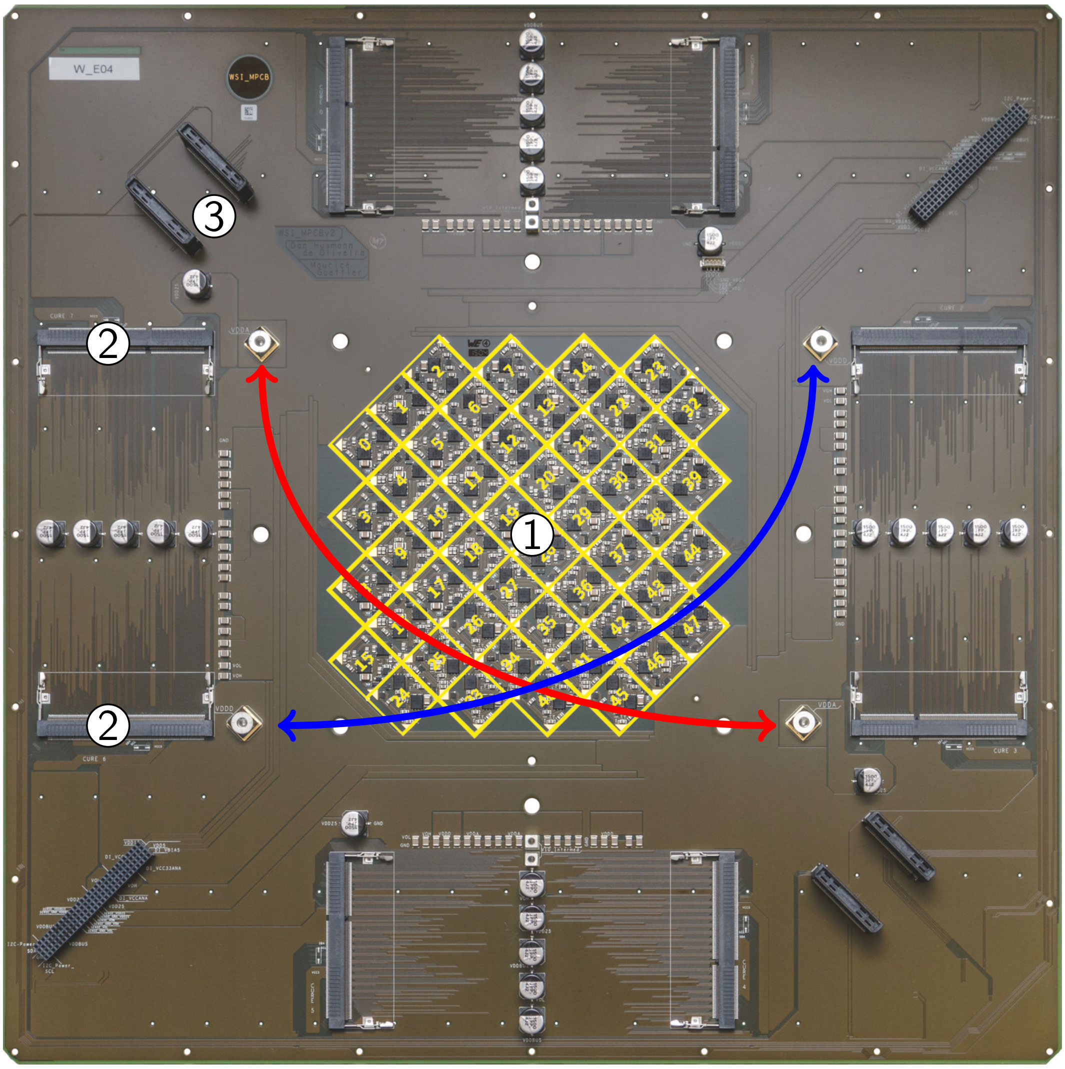

Figure 2.8.: A photograph of the top of the MainPCB (courtesy of Maurice Güttler [1]). The board has a length and width of 43cm. Visible in the center are the PowerFETs (Field Effect Transistors) (1) which switch the power supply of each reticle. These are controlled via the CURE boards. In yellow the corresponding Reticle and its position is marked. The CUREs are placed at the 8 central positions (2). The top-left and bottom right corner connectors (3) are for the AnaB boards. The main supply voltages V_{DDA} (red) and V_{DDD} (blue) are generated on the PowerIt and inserted at the marked screw connections.

2.2.3. Simple Wafer Resistance Model (SWRM)

To describe the reistances on such a wafer module, a model is needed. For that the circuit in Figure 2.9 can be used. This naive model will be referenced as SWRM (Simple Wafer Resistance Model) from here.

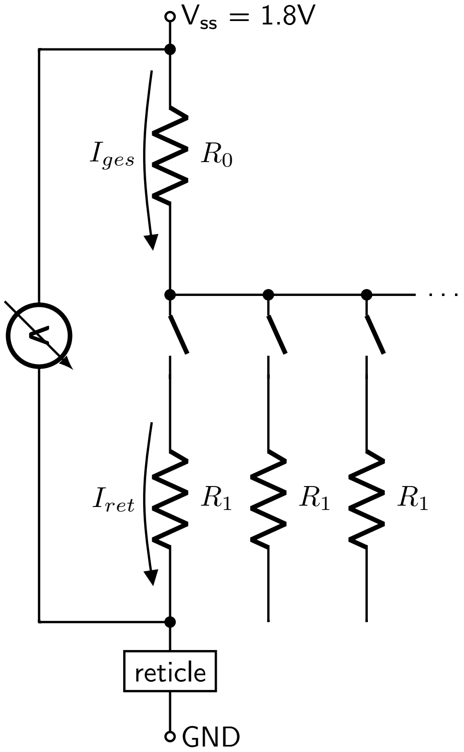

Figure 2.9.: model of the to measure resistances and their currents, R_0 describes the resistance of a connection between the PowerIt Output and up to the FET (depicted as switch), while R_1 is a Resistance between FET and Reticles. The measurement is done between Output Terminals on the PowerIt and pins on a Analog readout board

The SWRM circuit consists of two fixed resistance values and their respective currents as approximations of a real world system. It assumes that the connection to the nearest voltage connector is equal (electrically) for all reticles.

inside the code used for Regulation, Equation 2.16 will be used to create a lookup table, while Equation 2.20 will be used at runtime, for which Equation 2.18 and 2.19 are needed. In the SWRM, the current flowing through R_1 will be either 0 or a constant current I_{ret}. And the current through R_0 will change depending on the number of reticles that are powered n_{ret}

$$I_{ges} = n_{ret} \cdot I_{ret} \tag{2.17}$$

Therefore the voltage drop V_{dip} as measured by a voltmeter (see Figure 2.9) can be described with Equation 2.18

$$\begin{aligned} V_{\text{dip}} &= V_{R_1} + V_{R_0} \\ &= R_1 \cdot I_{\text{ret}} + R_0 \cdot I_{\text{ges}} \\ &= I_{\text{ret}} \cdot (R_1 + R_0 \cdot n_{\text{ret}}) \end{aligned} \tag{2.18}$$

$$V_{\text{dip}} = V_O - V_{\text{off}} \tag{2.19}$$

$$\Rightarrow V_O = I_{\text{ret}} \cdot (R_1 + R_0 \cdot n_{\text{ret}}) + V_{\text{off}} \tag{2.20}$$

3 Experiments

Now that the theoretical model is complete, experiments can be done to start checking that model and get results to use for in system components.

3.1. Experimental Setup

But before diving into the measurements ashort tour of both experimental setups. THe first setup was used during the calibration phase, while the secon setup was used for creating the regulation model.

3.1.1. Part 1

To calibrate a Powerit a setup is required, that can sweep the input voltage, as well as draw different current from the PowerIt (see Figure 3.1). For that a setup with a bench power supply an electronic load and an external voltmeter are used. Additionally a STM32-Discovery board and a RaspberryPi microcomputer were connected to flash new firmware onto the PowerIt.

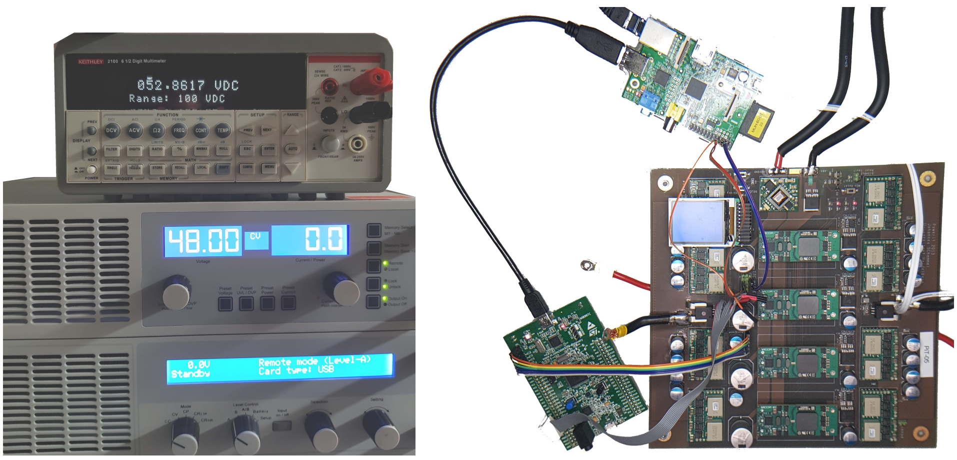

Figure 3.1.: Photographs of the first experimental setup. On the left side visible are a Keithley K2100 voltmeter (top), a PS9080 bench power supply (middle) and a EL9000 electronic load (bottom). On the right side visible are a PowerIt with connected STM32-Discovery board (left), and Raspberry PI (top). Also in the picture is the power supply connection (cables at top of PowerIt).

To now calibrate the board the bench supply could be controlled, to sweep through a voltage range, or in a similar fashio the electronic load could sweep through different current draw scenarios. This setup includes cable connections to voltmeter, power supply and load as to be able to control them with a piece of software.

3.1.2. Part 2

To obtain the required measurements for creating a regulation model the second setup was used (Figure 3.2).

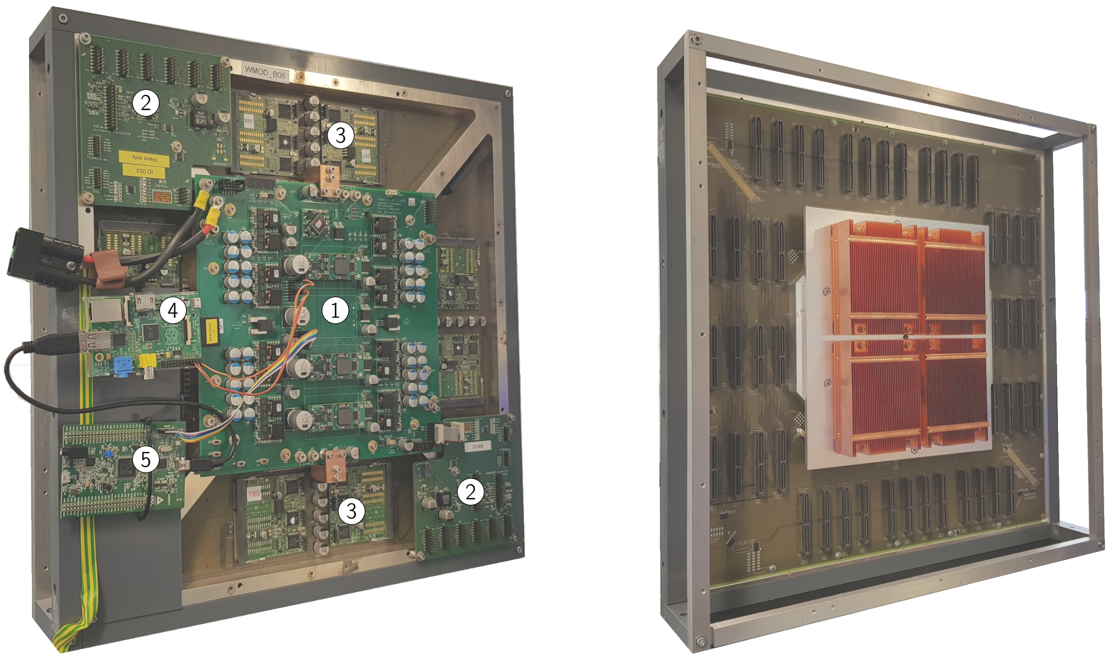

Figure 3.2.: Photographs of the second experimental setup. In this setup the Wafer system assembly was used. This module has a height and length of 50cm and a width of 15cm. The left side shows the back side of the assembly. Here are the PowerIt (1), CURE (3) and AnaB (2) boards mounted, as well as a RaspberryPi (4) and a STM32-Discovery (5). The right side shows the empty front side of the MainPCB and the wafer heatsink.

This setup is similar to a BrainScaleS wafer module as it exists inside the system. But in contrast to these systems there are no FPGAs, AuxPwr or FCP boards (reference [1],fig 2.2) The MainPCB has the PowerWafer embedded and is also connected to 8 CURE boards, 2 AnaBs and a PowerIt.

3.2. Characterization

The first experiments to run are the characterization of hardware behavior. These will then result in a PowerIt Calibration, which later then can be used as basis for creating a regulation method.

3.2.1. Sampling Time

First up was selecting an optimal number of cycles for which the adc will probe a to it connected pin, like described in subsection 2.1.1.

In this case the uncalibrated measurement of input voltage was taken as example, and repeated with each of the possible 8 settings.

To be able to compare a reference voltage measurement was taken with an external Voltmeter[1]. The resulting errors, from a set Voltage, can be seen in figures 3.3
Figure 3.3 contains the absolute error of the measured voltage compared to the theoretical, set input voltages. therefore the reference measurements (yellow), taken with an external Voltmeter, are not at 0. Also shown are the calculated gain errors, in case of all 8 settings.

Important to note is the relative error in only the 0th case, here the `cycleTime`-Setting was set to 0 and therefore the smallest available sampling time of 3 Ticks. This excludes 0 a possible value to use. All other measurements are within error margin of each other, and because a smaller time frame is preferred, the best value to use is 1, resulting in a measure time of 15 Ticks.

3.2.2. Voltages

Now that a sample time is chosen, it is possible to proceed with the voltage calibration measurements. Note, that measurements are expected to be less accurate, the more components are contained in their respective measurement circuit. Because small errors will accumulate and in e.g. the case of 48V's be amplified by a factor of 8.

48V Input

When looking at calibrating the input voltage (Figure 3.4), we can clearly see a relatively constant offset of $\approx$1V. In Figure 3.4 a polynomial fit of 2nd degree[2] is done and its coefficients extracted (code 1, line 9). These coefficients not only show an offset, but also some deviation in the incline and curve from the default values.

[1] Keithley K2100
[2] A Fit of second degree will be used in the complete calibration process

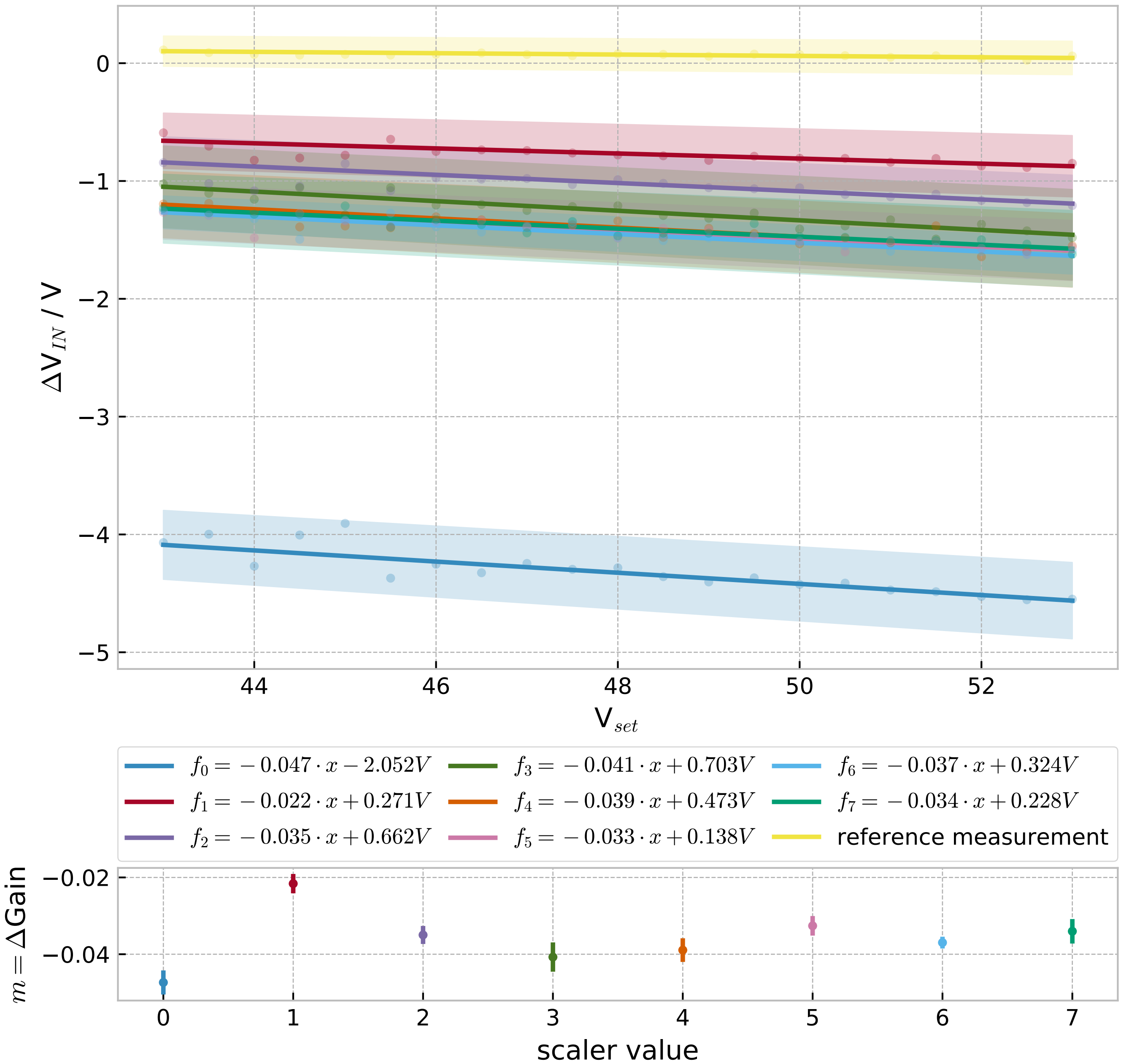

Figure 3.3.: Top: input difference from set voltage vs set voltage for different possible scaler values. Bottom: gain error of the linear fitted curves vs set scaler value (May 29th 2018, ≈32°C)

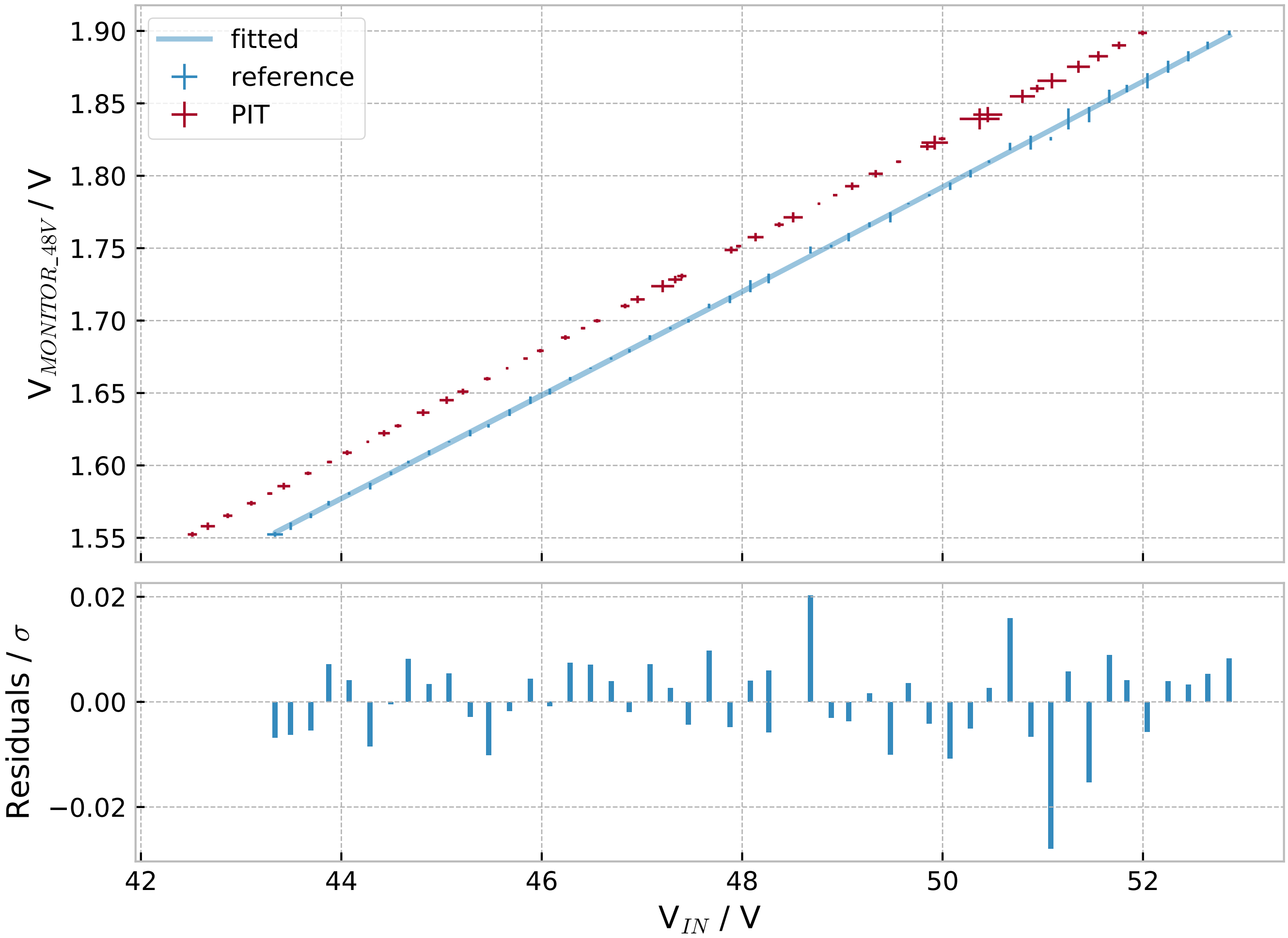

Figure 3.4.: Calibration of 48 V input voltage. Plotted are measured and reference vs the calculated vin voltage. The Calibration sweeps from 43.2 V to 52.8 V. The fit is of second degree and its inverse are the to use calibration coefficients. (fit:$(7.15 \pm 3.59) \times 10^{-5}\,\mathrm{V}^{-1} V_{\mathrm{IN}}^2 + (2.92 \pm 0.35) \times 10^{-2} V_{\mathrm{IN}} + (1.56 \pm 0.83) \times 10^{-1}\,\mathrm{V} = V_{\mathrm{MONITOR\_48V}}$)

9.6V Output

The 9.6V Calibration, in contrast, shows only a slight deviation of the internal values and the reference measurement, which results in a list of coefficients (??, line 7), very similar to those set in the theoretical defaults.

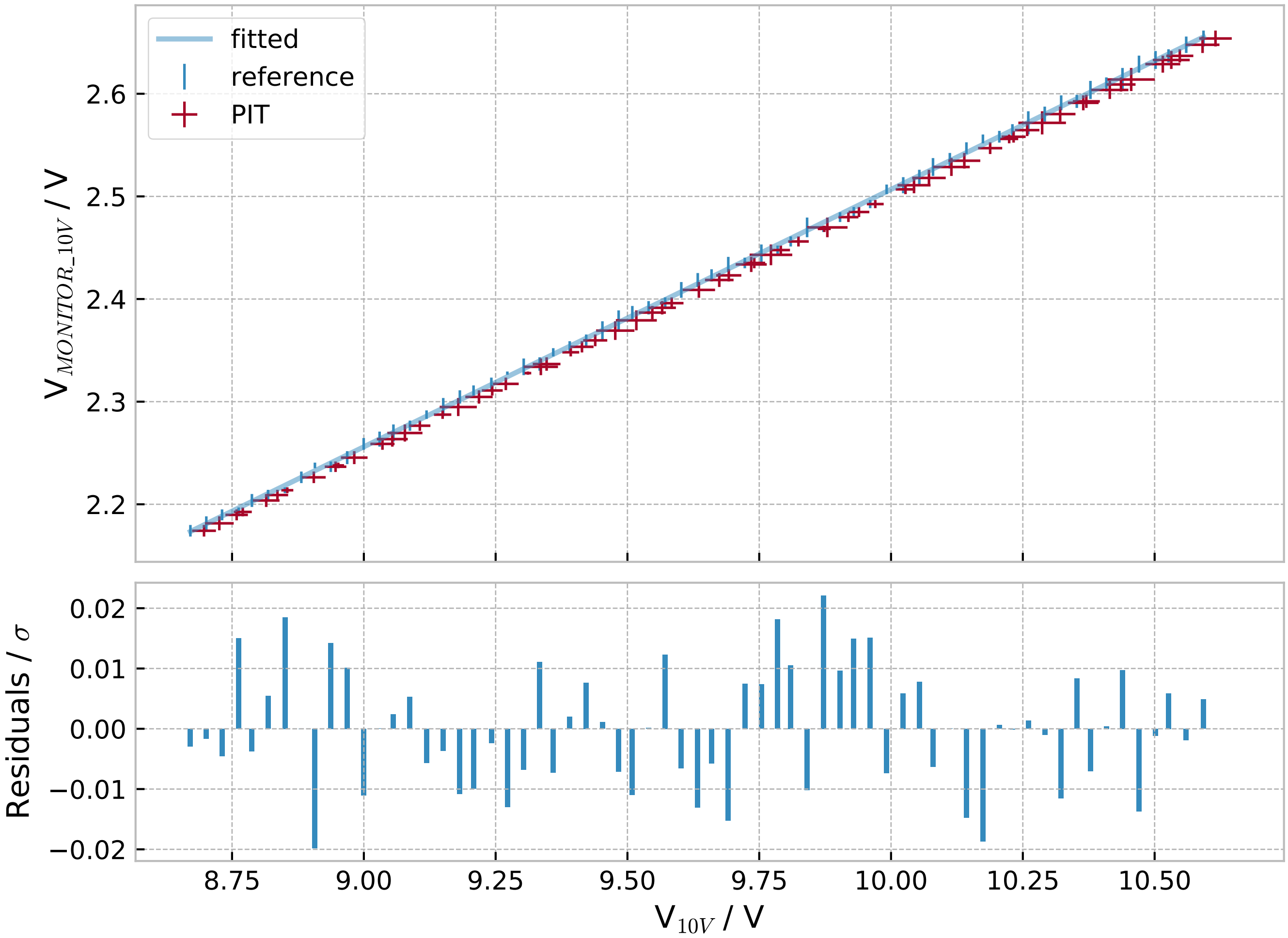

Figure 3.5.: Calibration of 9.6 V input voltage. Plotted are measured and reference vs the calculated vin voltage. The Calibration sweeps from 43.2 V to 52.8 V, and the supply mudules divide that into 8.64 V to 10.56 V. The fit is of second degree and its inverse are the to use calibration coefficients. (fit:$(-0.10 \pm 1.23) \times 10^{-3}\,\mathrm{V}^{-1} V_{\mathrm{10V}}^2 + (2.53 \pm 0.24) \times 10^{-1} V_{\mathrm{10V}} + = V_{\mathrm{MONITOR\_10V}}$)

This small difference is explained by the simple voltage division used as our circuitry, and no amplification, as for the input voltage circuit.

1.8V Output

The last Voltage to calibrate is divided into two domains, one for supplying the analog circuitry inside the wafer system, and one for the digital side. Each deliver between 1.5and 2.022V and each is settable by its own circuit (both as in Figure 2.4).

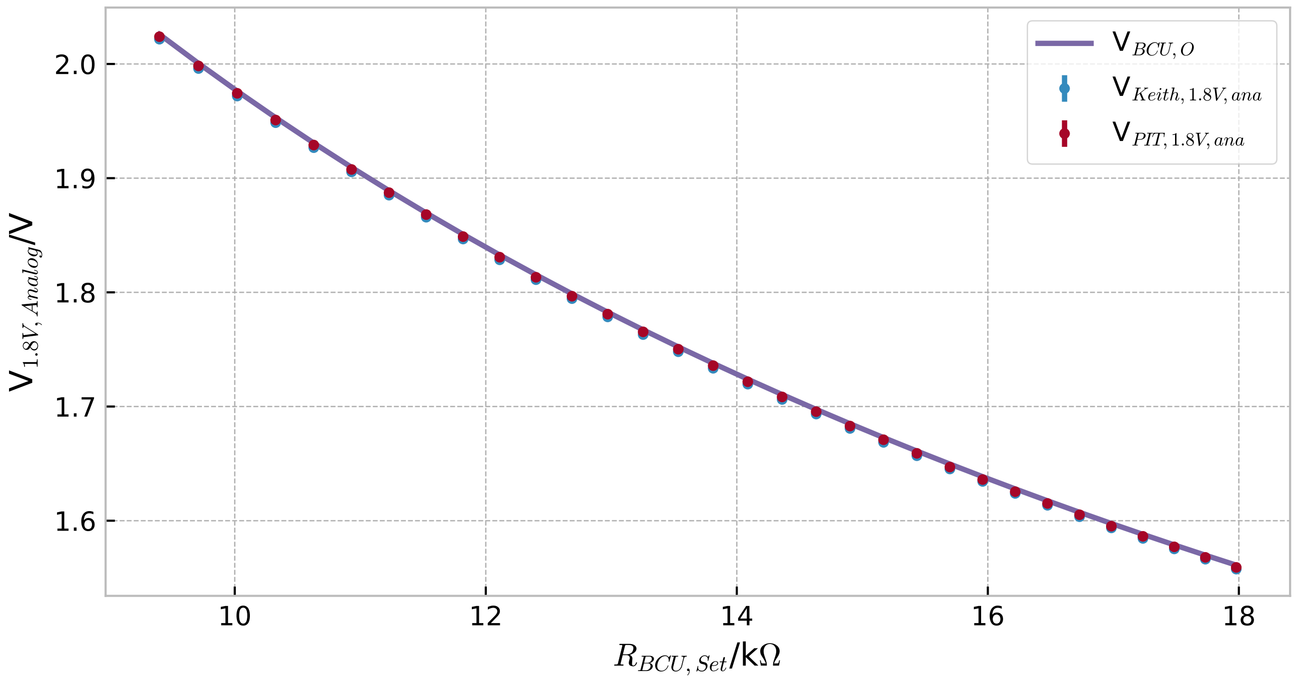

Figure 3.6.: Calibration: analog 1.8V Output voltage, plotted are external measurement and internal values vs set resistance at the BCU Voltage Module.

Visualized in Figure 3.6 is the analog domains calibration, showing nearly no difference in board and reference measurements. Mostly due to direct connection between created voltage and the STM-Chips pin.

3.2.3. Currents

With now calibrated Voltages, the next step is to measure the behavior of the current measuring circuits. Note that the 9.6V Output does in fact not have a include circuit for measuring its current draw, and that this number will be obtainable from all other (calibrated) measurements.

48V Input

This experiment will calibrate the 48V input current. In it the current drawn by the PowerIt sweeps over a range from 0 A to 20 A.

In Figure 3.7 quite a gap between observed and measured values can be seen. This is most likely a gain error, which would result in a error in m_2, as observed. And the fitted curve has the following parameters:

$$\begin{aligned} V_{\mathrm{MONITOR\_48I}} &= m_0 + m_1 \cdot I_{\mathrm{IN}} + m_2 \cdot I_{\mathrm{IN}}^2 \\ m_0 &= (2.64 \pm 1.01) \times 10^{-3}\,\mathrm{V} \\ m_1 &= (5.63 \pm 0.25) \times 10^{-3}\,\mathrm{V\,A^{-1}} \\ m_2 &= (1.36 \pm 0.13) \times 10^{-4}\,\mathrm{V\,A^{-2}} \end{aligned} \tag{3.1}$$

from which the inverse will used for calibration inside the PowerIt.

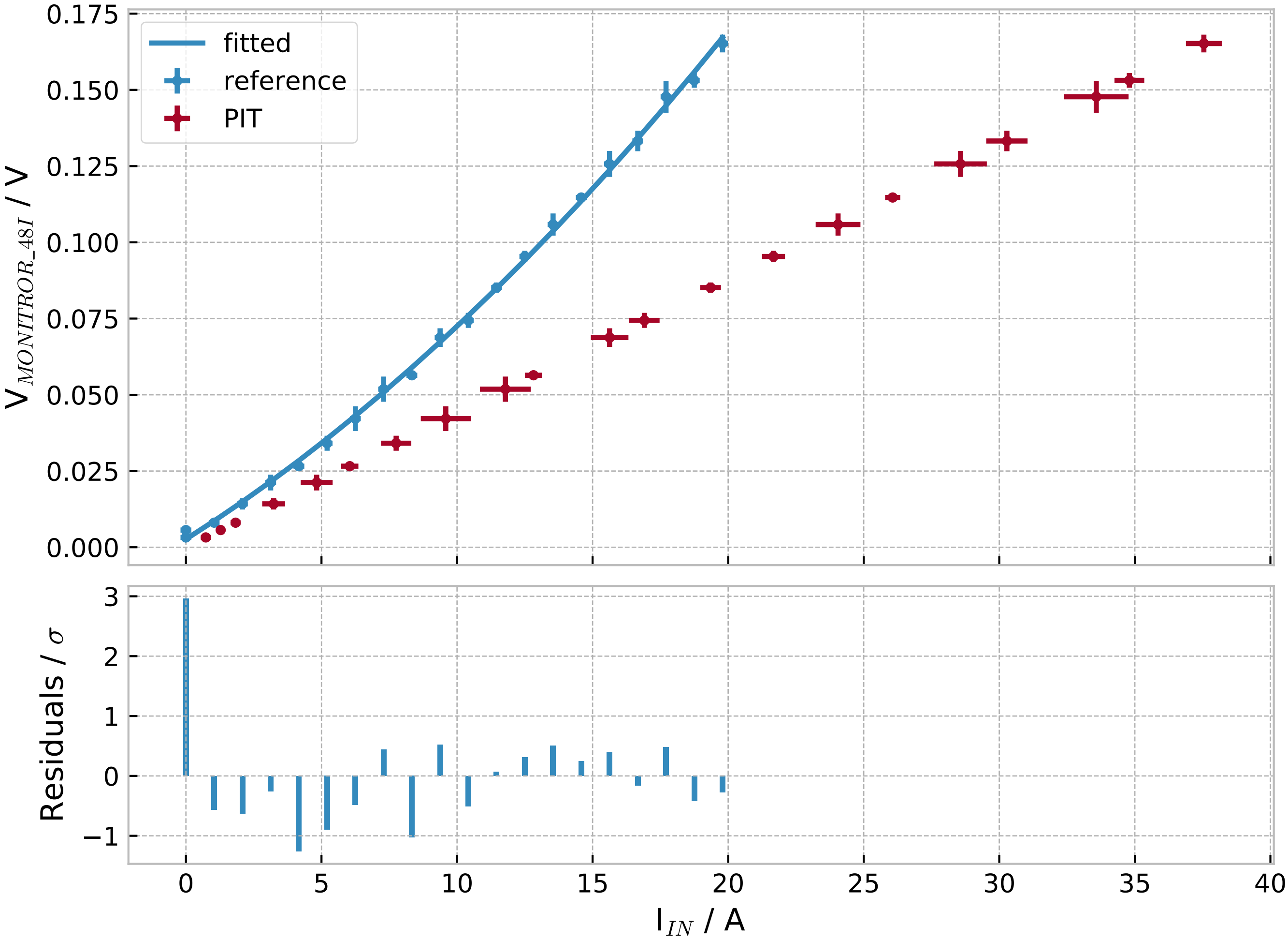

Figure 3.7.: Calibration of 48 V input current. Plotted are measured and reference current vs the calculated pin voltage. The Calibration sweeps over 0 A to 20 A. The fit is of second degree and its inverse are the to use calibration coefficients.

1.8V Output

For the calibration experiment of both 1.8V output currents, the current draw ranged from 0 A to 90 A. Observed were the values in Figure 3.8. Visible is a different incline of internal measurement and reference.

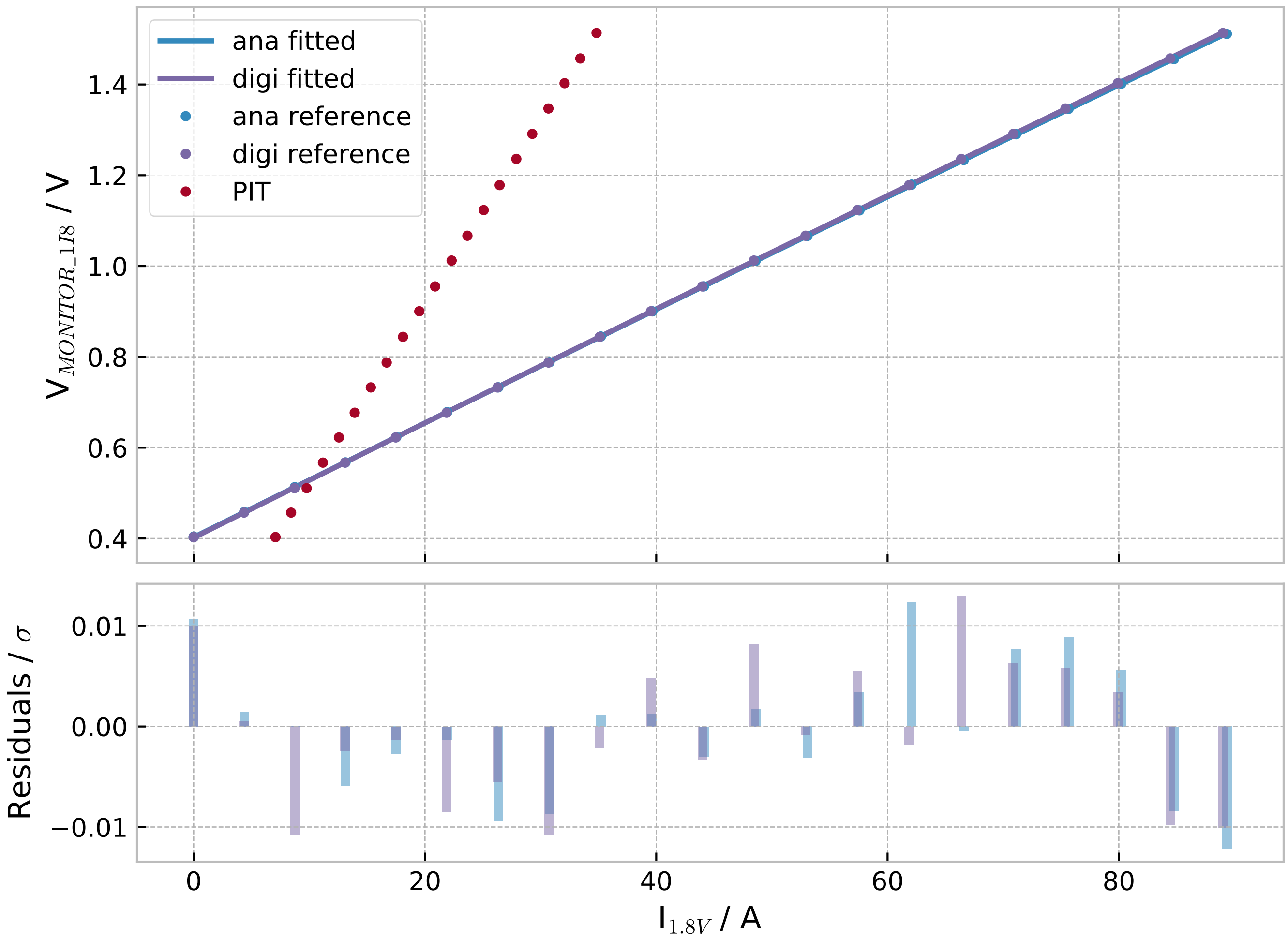

Figure 3.8.: Calibration of 1.8 V output current for both digital and analog. Plotted are measured and reference current vs the calculated pin voltage. The Calibration sweeps over 0 A to 90 A. The fits are of second degree and their inverse are the to use calibration coefficients.

The fitted curve for the analog side were:

$$\begin{aligned} V_{\text{MONITOR\_1I8\_ANA}} &= m_0 + m_1 \cdot I_{\text{1.8V, ana}} + m_2 \cdot I^2_{\text{1.8V, ana}} \\ m_0 &= (4.03 \pm 0.00) \times 10^{-1}\,\text{V} \\ m_1 &= (1.26 \pm 0.00) \times 10^{-2} \\ m_2 &= (-2.33 \pm 0.27) \times 10^{-6}\,\text{V}^{-1} \end{aligned} \tag{3.2}$$

, while the digital side had quite similar values of:

$$V_{\mathsf{MONITOR\_1I8\_DIGI}} = m_0 + m_1 \cdot I_{\mathsf{1.8V,\ digi}} + m_2 \cdot I^2_{\mathsf{1.8V,\ digi}} \tag{3.3}$$
$$m_0 = (4.02 \pm 0.01) \times 10^{-1}\,\mathrm{V}$$
$$m_1 = (1.27 \pm 0.00) \times 10^{-2}$$
$$m_2 = (-1.90 \pm 0.31) \times 10^{-6}\,\mathrm{V}^{-1}$$

This also show, that both parts are so similar in bahavior, that a single sides observations would have sufficed.

3.3. 1.8V Regulation

As Described beforehand the Output Voltages for both analog and digital can be adjusted to some degree and therefore we can compensate for the dropoff occurring between PowerIt Output Terminals and Reticles.

To run any test with the PowerWafer, the patterns in Figure 3.9 were used. Tere are two reasons for that, firstly these patterns distribute the current draw in a regular fashion as to distribute the load between the connectors. Secondly, when powering Reticles all of the energy is converted into heat, via the ohmic resistors.

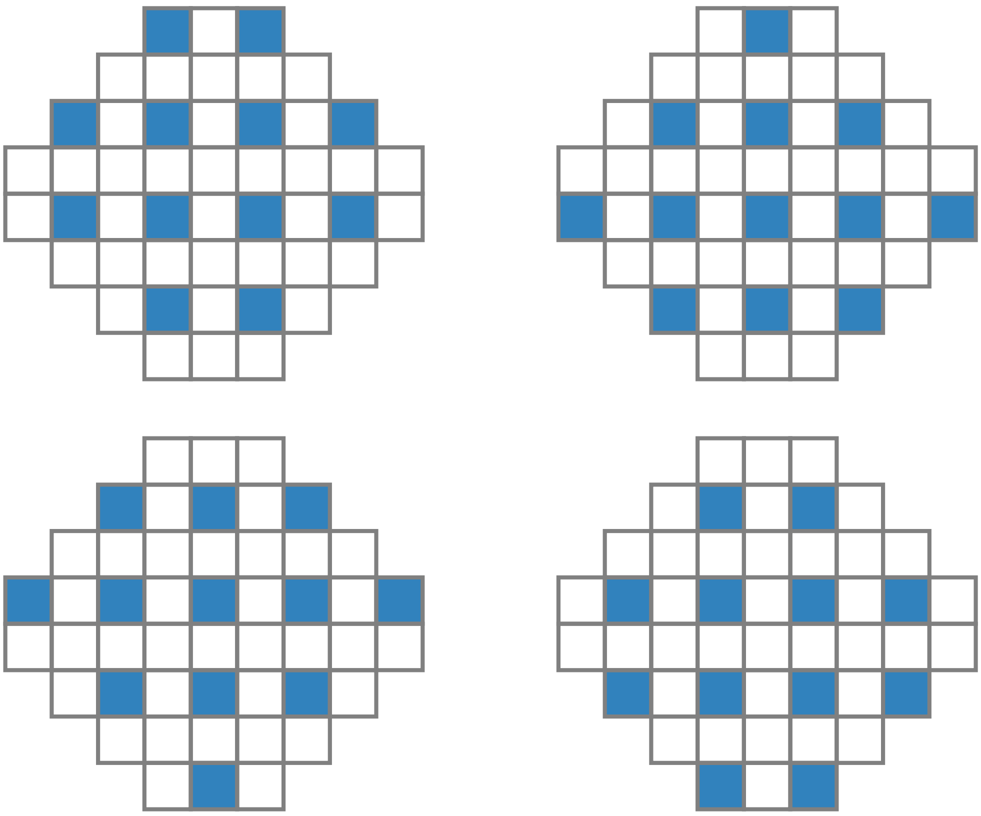

Figure 3.9.: Used regular patterns for current tests on PowerWafer

And although the copper heat sink and fans (see Figure 3.2), should be able to handle this heat in theory, when grouping together reticles and powering them, the dissipation does not suffice. The internal temperature probes (between heatsink and wafer) register well above 50 °C, when grouping 3 or more reticles.

3.3.1. Characterization of Dropoff

Wanting to observe and characterize the voltage drop, first the connections between PowerIt and Reticles can be measured with the in Figure 2.9 described connections, which in actuality are the PowerIT Terminal and corresponding analog readout pin on a Analog readout board.

To use the PowerWafer for testing one of the patterns in Figure 3.9 will be used, each pattern has a approximate current draw of 120A and will distribute heat and draw per terminal evenly.

In Figure 3.10 a single reticles (#40) voltage drop for different Current Draws is visualized. A relatively linear trend and residuals of a trigonometric behavior can be observed (most likely the result of the inaccurately measurable current draw, which here is done inside the PowerIt).

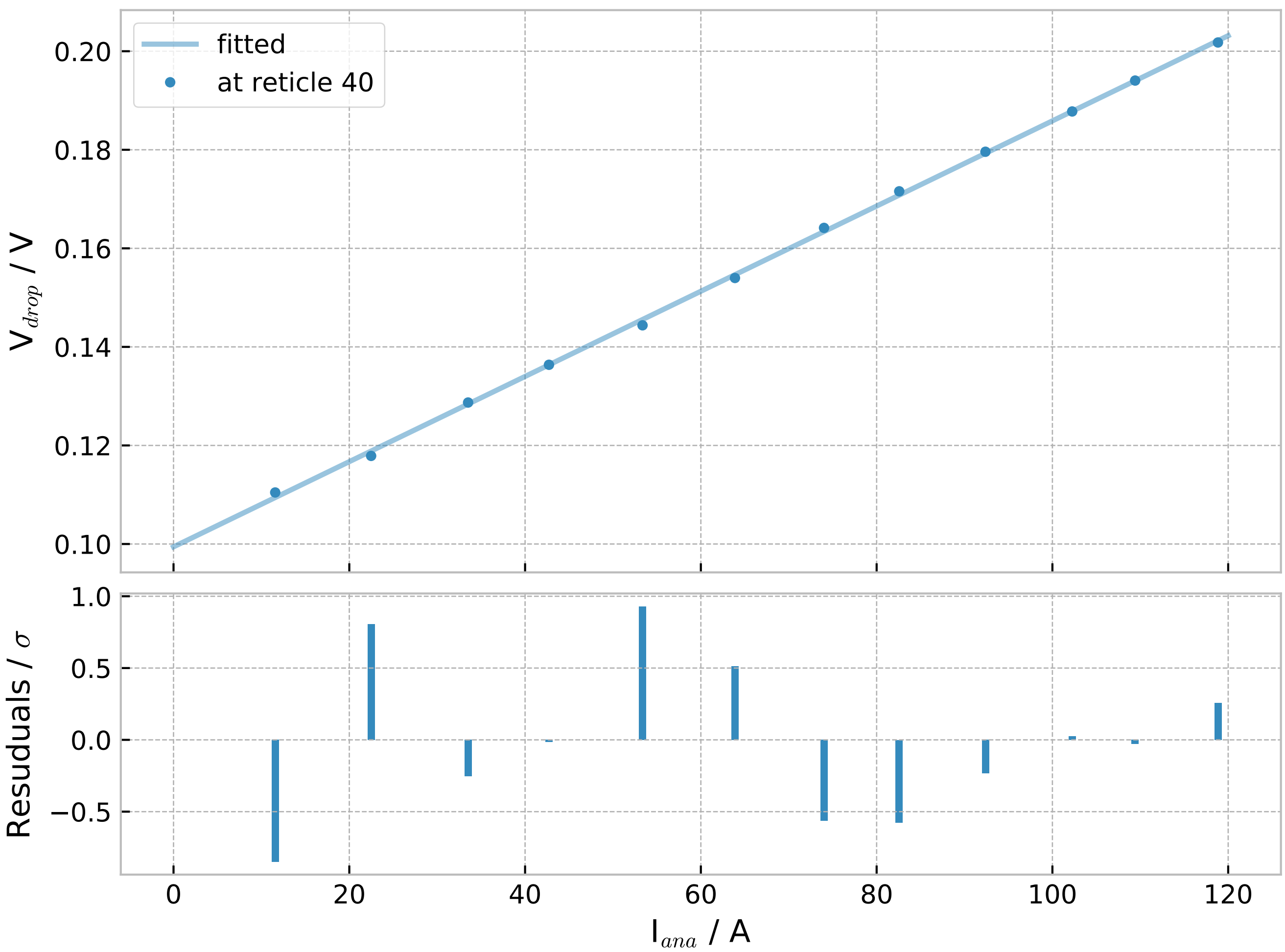

Figure 3.10.: Voltage drop observed between PowerIt and HICANN, each point represents a state after enabling additional Reticles on the PowerWafer (right upper wafer in Figure 3.9)

Here a Voltage Drop vs. Current draw of the wafer shows a linear behavior and therefore can be regulated on basis of the current measurement done by on board Measurement circuit.

3.3.2. Numerical-Correction (Regulation)

The initial idea, to approach the correction of this dropoff is a Numerical: the SWRM (subsection 2.2.3) and its corresponding Equations can be applied here. Equation 2.16, which maps the measured output current to a corresponding potentiometer setting, requires the Dropoff to be linear, which was observed.

To apply this approach, two assumptions need to be made:

- all reticles have the same current draw (already not accurate, see Figure 3.10)
- all reticles experience the same voltage drop (as observed for reticle 40)

and the following four values are required, before a regulation can be attempted:

- I_{ret}, the current draw of a single reticle,
- R_0, the resistance between PowerIt and FET,
- R_1, the resistance of a single Reticle
- V_{off}, the wanted Voltage at a Reticle

To get a representative value of I_{ret} for use in the SWRM, the mean of all reticles current draw was taken (Figure 3.11):

$$I_{\text{ret,mean,corr}} = (9.9089 \pm 0.6049)\,\text{A} \tag{3.4}$$

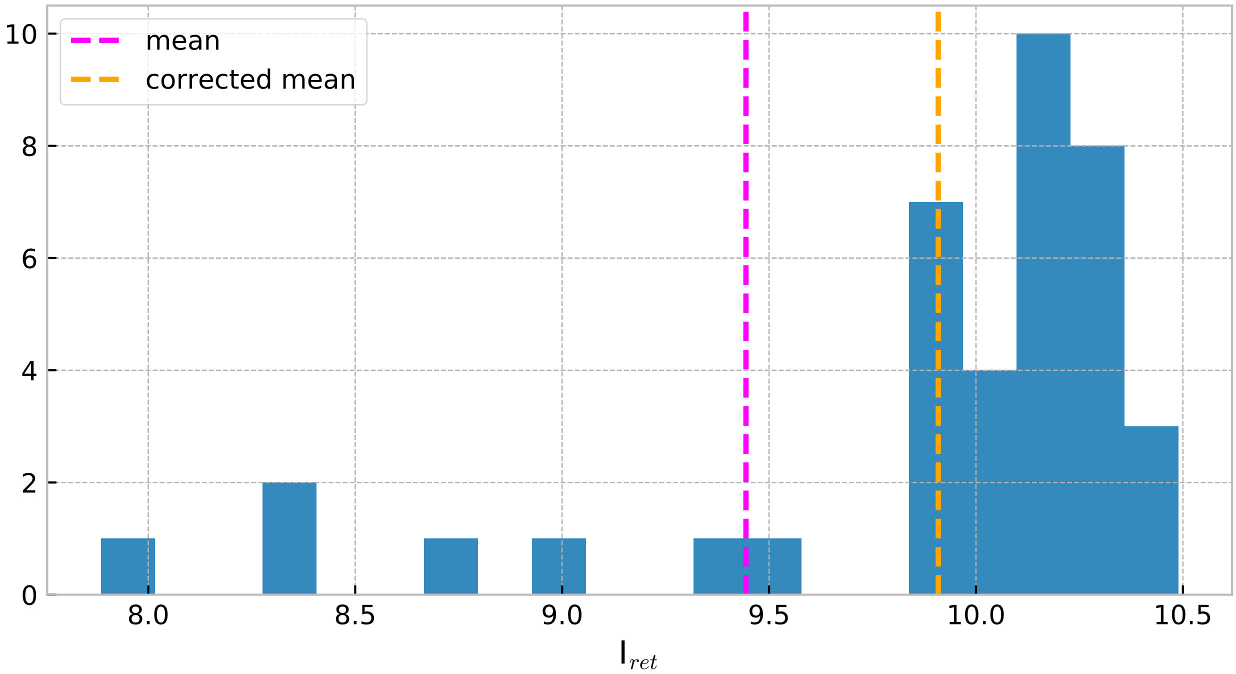

Figure 3.11.: Distribution of analog current draw for all reticles on the PowerWafer (which were possible to measure → ??)

The Figure 3.11 was obtained by measuring the increase in current draw for each reticle, for each of the 4 patterns (Figure 3.9).

To obtain R_0, the pattern in Figure 3.12 was used to take measurements for both the Neighborhood as well as the Farthest Reticles.

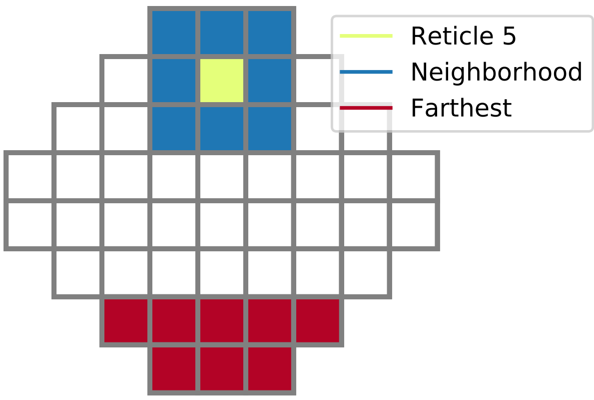

Figure 3.12.: Reticles used to determine correlation between distance and Voltage Drop

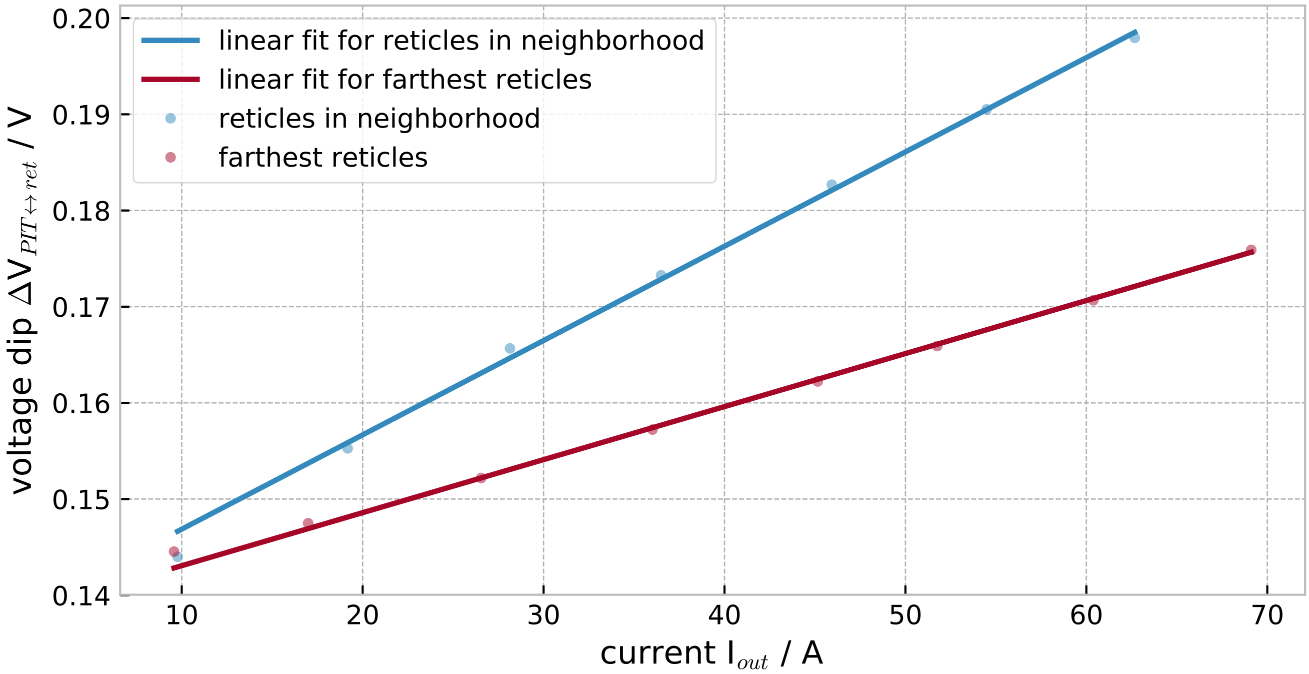

Figure 3.13.: Voltage drop vs current for both Reticles in direct neighborhood and farthest possible Reticles

From Figure 3.13 it is possible to see that the distance between reticles that are used gives different behavior of the voltage drop. Both Inclines happen to be the extreme cases, while either being completely uncorrelated, the case for farthest Reticles, or being directly correlated by their distance, here observable for the neighboring Reticles.

Therefore we obtain two values for R_0:

$$R_{0,\text{neighbor}} = (7.1278 \pm 0.1567)\,\text{m}\Omega \tag{3.5}$$
$$R_{0,\text{farthest}} = (4.0079 \pm 0.0537)\,\text{m}\Omega \tag{3.6}$$

from the same measurement it is also possible to extract R_1 by extrapolating to 0, which results in:

$$R_{1,\text{neighbor}} = (14.1708 \pm 0.1779)\,\text{m}\Omega \tag{3.7}$$
$$R_{1,\text{farthest}} = (14.2218 \pm 0.1503)\,\text{m}\Omega \tag{3.8}$$

here the values obtained are within error margin of each other.
So applying these Values, the following behavior for regulation can be visualized:

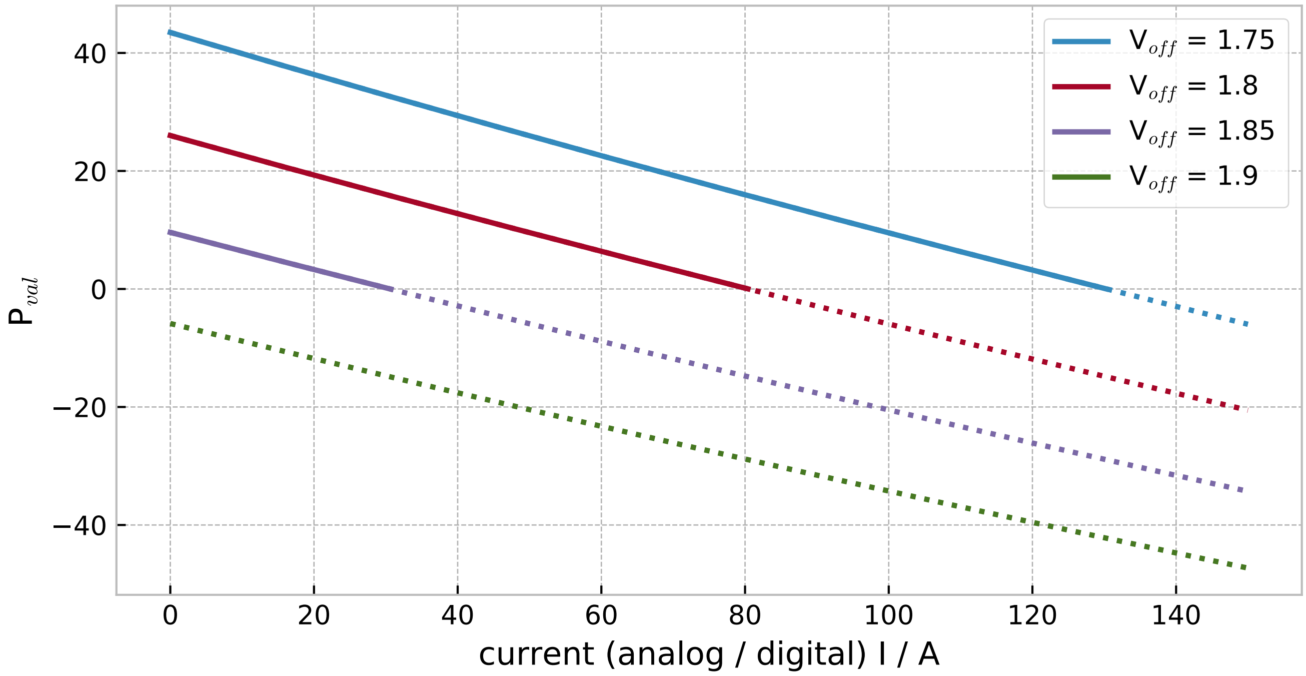

Figure 3.14.: Possible P_{val} curves after SWRM, dotted lines represent not achievable values

The in Figure 3.14 visualized values show the theoretical P_{val} for the corresponding Current, while all dotted parts depict the values which would be needed to achieve full correction at the Reticle level. Note that the 1.8V regulation, should fail at about 80A of current draw.

Now that the SWRM is applicable, what about the DWRM, which removes the assumption of a equal voltage drop per reticle, applying an offset to the initially observed voltage of each reticle.

To account for that, the voltage drop per reticle, in a single reticle power state, was observed:

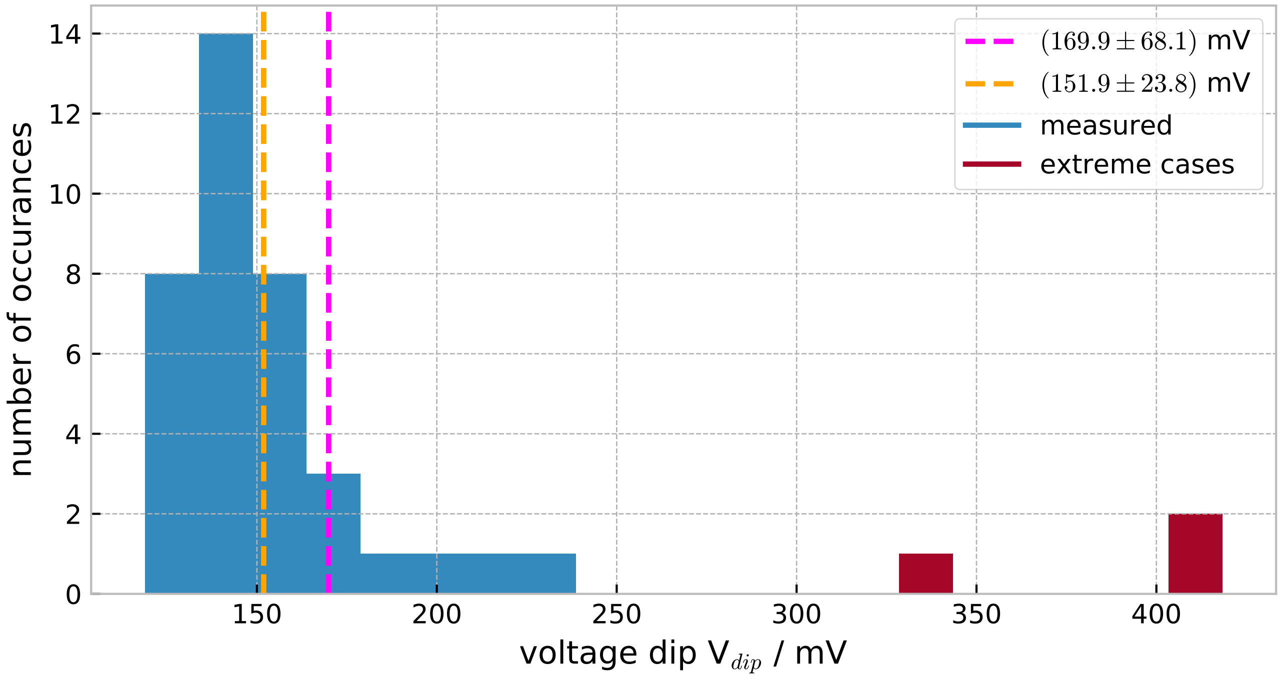

Figure 3.15.: Initially observed voltage drop, red values are ignored for corrected mean

and a mean of:

$$V_{\text{dip,mean,corrected}} = (151.8811 \pm 23.8138)\,\text{mV} \tag{3.9}$$

can be observed.
Figure 3.16 shows how those Voltages are Distributed over the complete PowerWafer. All white Reticles are not measurable, and those colored in Red and Yellow are the outliers in Figure 3.15. Note that in a deployed, working, Wafer System inside BrainScaleS the middle two Reticles (19 & 28) are not used and also give grounds to ignoring the outliers.

This results in a distribution, which when combined with the spread of R_0 from Figure 3.13, gives an approximate range for all reticles voltage drop at a given current draw (**??**). The last values that were measured, came from the CURE boards connected to each reticle. The voltages obtined from these boards, can be compare to the manually obtained voltages vie AnaB pins. In Figure 3.17 these voltages are visualized, in comparison to the AnaB voltages.

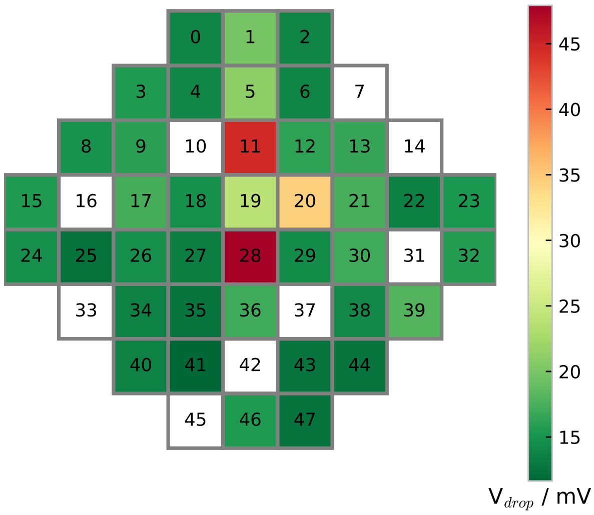

Figure 3.16.: V_{drop} distribution over full Power Wafer; White have no measurement; Red an Orange are marked red in Figure 3.15

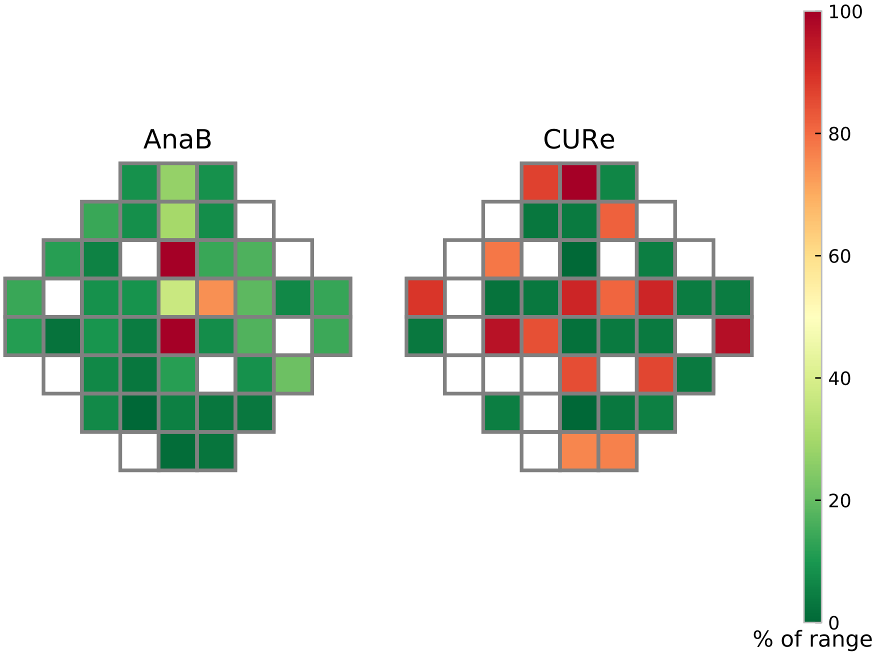

Figure 3.17.: Qualitative comparison of AnaB and CURe measured voltage drop. Colors indicate their respective relative values for each measurement. White reticles have no measurement.

This comparison shows no discernable relation between both measurements. This could be the result of not correctly calibrated CURE boards, or at least hints to some problem with the measurement.

4 Results

In this chapter all results from the experiments, as well as reasons will be discussed.

4.1. Calibration

This calibration process yielded some workflows for use inside the system as well as calibration values for the used PowerIt.

4.1.1. Calibration-Database

The obtained calibration values for the in these experiments used PowerIt, are combined in code 1.

```yaml
---
id: '0x280029000F51333332343638'
name: B05
poly18iana: [-31.5155, 78.516, -0.0688]
poly18idigi: [-31.3536, 78.3701, -0.196]
poly18i: [-31.4396, 78.443, -0.1324]
poly48i: [-0.1765, 153.0021, -204.1858]
poly10v: [0.6348, 3.459, 0.1118]
poly48v: [-4.5248, 33.3195, -1.6167]
poly18v: [0.0234, 0.9728, 0.0072]
```

Code 1: PITDB entry for B05 PowerIt. `id` is obtained by the firmware and unique to each STM32Chip. The `name` corresponds to the label on each PowerIt. All `poly*` are all polynomial coefficients in order of 0th degree to 2nd degree.

And to compare, the values in code 2 are theoretical values, obtained from all equations in chapter 2.

```
---
uuid: 'default'
name: 'Bxx'
poly18i: [-3.0, 25.0, 0.0]
poly48i: [0.0, 227.27, 0.0]
poly10v: [0.0, 4.0, 0.0]
poly18v: [0.0, 1.0, 0.0]
poly48v: [0.0, 27.386, 0.0]
```

Code 2: Default PITDB entry for any PowerIt. All `poly*` are all polynomial coefficients in order of 0th degree to 2nd degree.

4.1.2. Accuracy

To obtain an accuracy for the internal measurements, the experimental sweeps can be repeated after calibration. One example of a calibrated measurement can be seen in Figure 4.2.

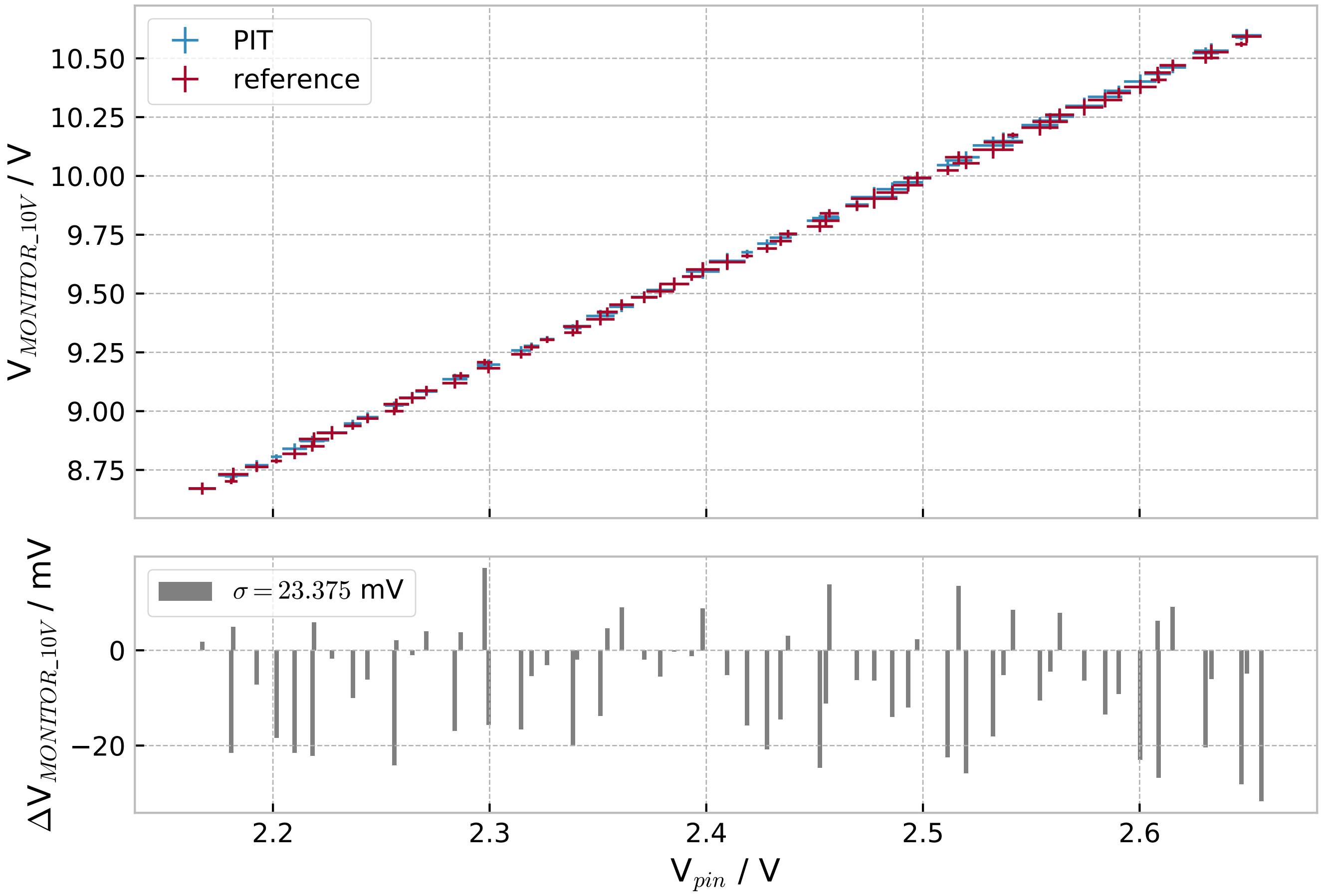

Figure 4.2.: Voltages after calibration. Sweep from 43.2 V to 52.8 V input voltage resulting in a range from 8.64 V to 10.56 V. The errors in the bottom diagram show the differences between reference and PIT values.

This repeats the calibration measurement for 9.6 V. Here quite similar values can be observed, with a maximum ΔV of around 31.676 mV. It is also possible to see a systematic error in Figure 4.2. This error could be corrected, but requires quite some time investment. It would allow for a reduction of ΔV, up to a value of 24.456 mV.

This result is similar to others, and for all it would be possible to achieve a bit better fits.

4.2. Regulation

4.2.1. Resulting Observation

To verify the regulation is working and to see if the prediction in Figure 3.14 is correct new values were measured. THese Values are the voltages with regulation enabled at different Reticles (see Figure 4.3).

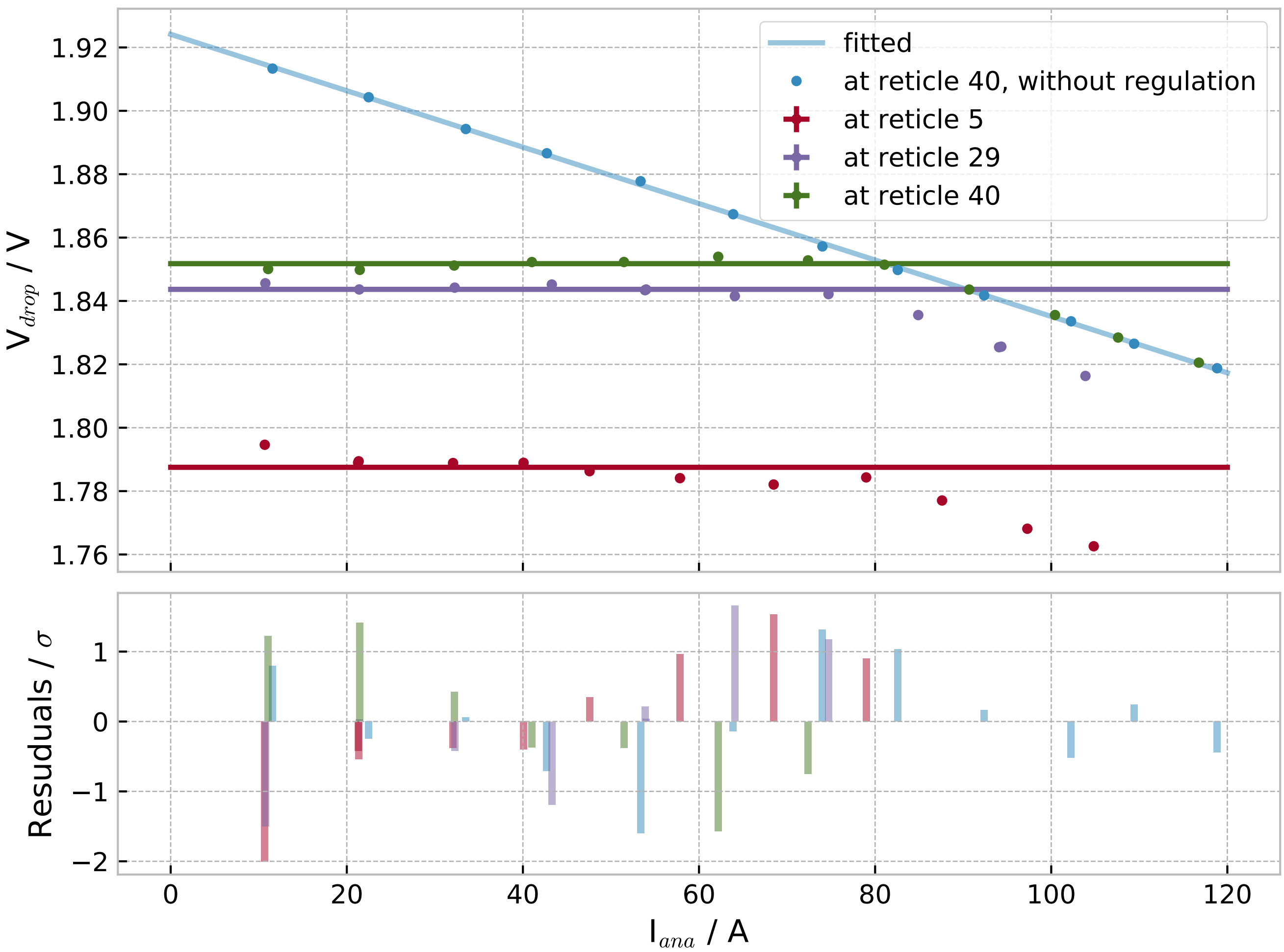

Figure 4.3.: Observed AnaB voltages after regulation at multiple reticles. Reticle #40 shows the best-case scenario with the least amount of V_{drop}. Reticle #5 is a worst-case scenario, with the highest V_{drop} while still being a usable reticle.

In this figure three different reticles (#5, #29 and #40) were measured. Observable is, that firstly the regulation, which was set to achieve 1.8 V is working until I_{ana} is at about 80 A. There the minmal potentiometer setting is used. From here further regulation, with the same hardware, is impossible.

Secondly the voltages for different reticles is different and not equal. This was one of the assumptions in the SWRM. To describe that behavior a distance based model (subsection 4.2.2: DWRM) could be the solution.

And third, under the assumption of a constant fit (up to $I_{ana} \approx 80$ A) a systematic error can be observed.

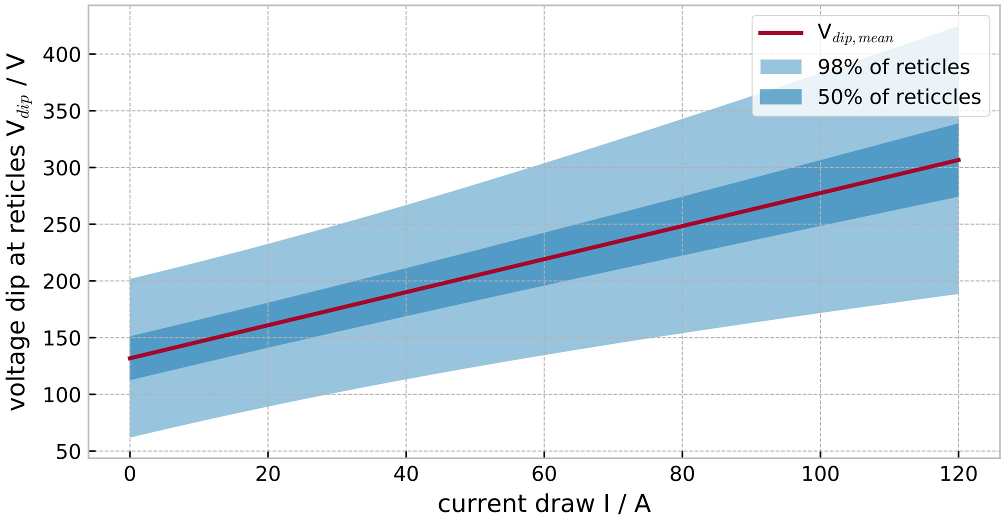

Figure 4.4.:

4.2.2. Distance Wafer Resistance Model (DWRM)

Although the through SWRM gained functions approximate the real world, it is not exact enough. In a wafer, the distance between reticles and voltage connector (see Figure 2.8) are resulting in additional resistance.

Therefore the DWRM could be adapted. Circuit 4.5 visualizesa model, in which each different distance from the voltage connector, is classified with an additional resistance.

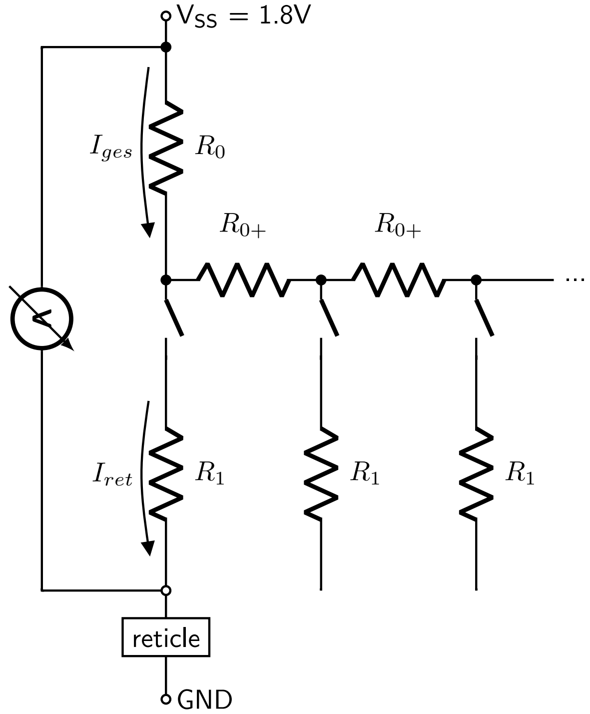

Figure 4.5.: Modified model of the to measure resistances and their currents. Similar to SWRM R_0 describes the resistance of a connection between the PowerIt Output, up to the FET (depicted as switch), while R_1 is a Resistance between FET and Reticles. But additionally R_{0+} described a Resistance, that depends on the distance between reticle and voltage connector. The measurement is done between output terminals on the PowerIt and pins on a Analog readout board

With this model the voltage is now expected to change depending on the reticles distance instead of being the same. The distances inside a wafer are visualized in Figure 4.6

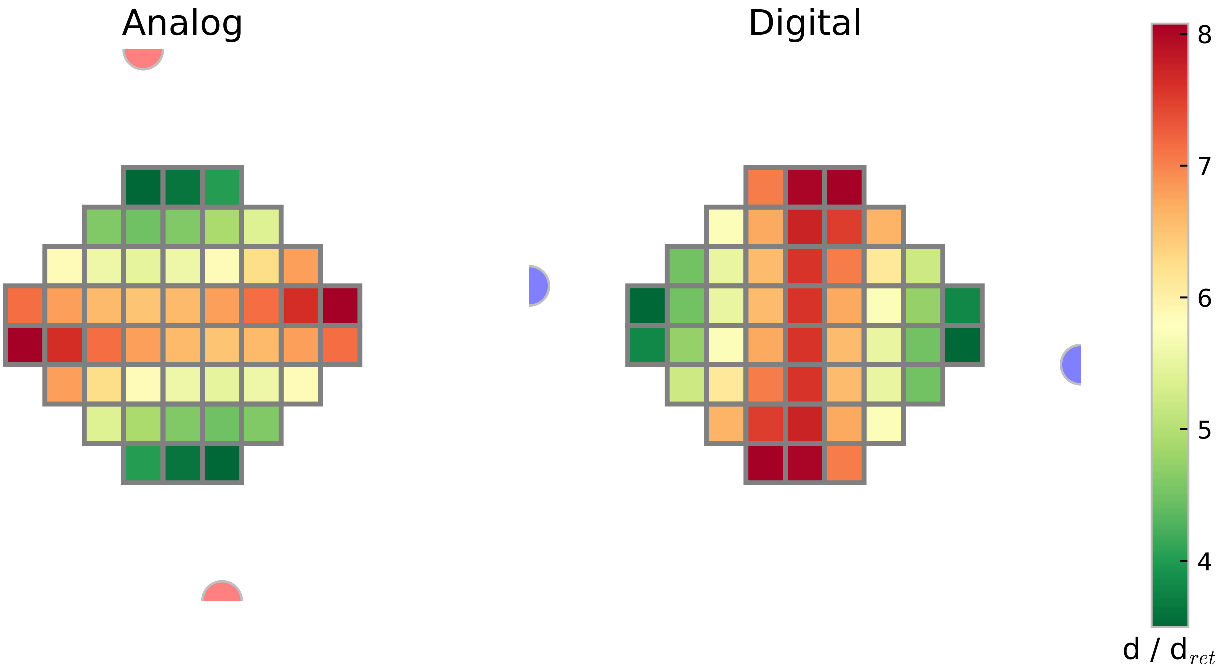

Figure 4.6.: Distances of reticles to the nearest voltage supplying connection for DWRM, distance is in reticle-side length

Additionally this model is a better fit to the already observed voltage distribution in Figure 3.16.

5 Outlook

All in all the set goals were achieved.

While all of the measurements could be calibrated they can still be fine tuned. As shown in Figure 4.2, the error of a calibrated measurement is not quite minimal. In the future it would be possible to make these even more accurate, either by using a different method for calculating, which is not based on second degree polynomials. Or by further calibration, as mentioned in the results chapter.

The voltage distribution, as described in figures 3.15 and 3.16, was quantified and the SWRM could be used for creating a worst-case V_{drop} distribution as seen in Figure 4.4. Therefore a first iteration of a usable regulation mechanism could be implemented and verified (see Figure 4.3). This mechanism allows for a certain degree of regulation until a current threshold is reachd. This threshold was also agreeing with a beforehand calculated value of around 80 A

For further developing this the more complex DWRM could be used. This would allow for a more accurate regulation, that would narrow down the worst-case scenario of Figure 4.4. For that model to work, each experiment run on a wafer, in the system, would require a simulation of the distribution of voltage between the used reticles. As to minimize the maximum difference in voltage drop. This could also factor in the number of active HICANNs per reticle.

Additionally the current threshold is restricted by the internaly used resistor chain (described in Figure 2.4). If the minimum resistance of that circuit were to be changed, the threshold would move up in current.

I Appendix - Firmware

I.1. Virtual Memory Mapping

THe biggest Change done to the Firmware was the implemetation of a new communication protocoll. This protocoll uses the following table as reference

I.2. How to calibrate a PowerIt Board

The Calibration process is based on the PItSTOP Python scripts[1]. These are split into `server` and `aggregator`. While the Server is handling the translation between raw I^2C data, and the JSON formatted result, the Aggregator takes this JSON and calculates a calibration.

Using the script any one of the following Values can be tested and calibrated:

- Input Voltage (`pitstop.Aggregator.test_v_48()`)
- Input Current (`pitstop.Aggregator.test_i_48()`)
- 9.6V Output Voltage (`pitstop.Aggregator.test_v_10()`)
- 1.8V Output Voltage (`pitstop.Aggregator.test_v_18()`)
- 1.8V Output Current (`pitstop.Aggregator.test_i_18()`)

I.2.1. Setting up the Test Environment

The simplest way to setup an environment consists of cloning the PItSTOP project on a client:

```
> git clone https://url.to.pitstop
```

then substituting the `rsync` target:

```
all:
    rsync --progress ./*.py /remote.url/
```

, to be your server (should be a RaspberyyPi connected to the PowerIt)

[1] PItSTOP Repo

addr	name	type	size	perm
0x00	onmask	byte	1	rw
0x01	offmask	byte	1	rw
0x02	anapot	9bit	2	rw
0x04	digipot	9bit	2	rw
0x06	polyFit.V48	float arr	12	rw
0x12	polyFit.I48	float arr	12	rw
0x1e	polyFit.V8	float arr	12	rw
0x2a	polyFit.V18	float arr	12	rw
0x36	polyFit.I18	float arr	12	rw
0x42	polyFit.T	float arr	12	rw
0x4e	sampleTicks	byte	1	rw
0x4f	V_out	float	4	rw
0x53	TEMP_SENSOR	float	4	r
0x57	EXT_AIN	float	4	r
0x5b	MONITOR_48V	float	4	r
0x5f	MONITOR_48I	float	4	r
0x63	MONITOR_8VBUS	float	4	r
0x67	MONITOR_8IBUS	float	4	r
0x6b	MONITOR_8V_0	float	4	r
0x6f	MONITOR_8V_1	float	4	r
0x73	MONITOR_8V_2	float	4	r
0x77	MONITOR_8V_3	float	4	r
0x7b	VDD_1V8_ANA	float	4	r
0x7f	VDD_1V8_IOUT_ANA	float	4	r
0x83	VDD_1V8_DIGI	float	4	r
0x87	VDD_1V8_IOUT_DIGI	float	4	r
0x8b	CommitHash	float	4	s
0x8f	CommitDirtyFlag	byte	1	s
0x90	STM32UUID	96bit	12	s

Figure I.1.: memory mapping of the packed struct moved over i2c, `addr` is the address to use, `type` is the c++ type, `size` is in bytes and `perm` denotes read-writability. writability

Figure I.2.:

I.2.2. Running a Test

Runnig the test requires the following commands
Serverside:

```
> python server.py
```

Clientside:

```
> python aggregator.py
```

Now just following the instructions given, the selected test can be run:

```
Setting up calibration test for {}
Please be sure to:
 - connect the {} to the RaspberryPi running server.py.
 - connect the PowerIt to the RaspberyPi as described in the
  ↪  documentation
 - and be sure to connect the {} to the {} Terminal.

Continue (y/N): y

What is the Name given to the connected PowerIt? [Bxx]: B05
```

The result will consist of two diagrams one without calibration and one with. It will also write the newly obtained calibration data into `pitdb.yaml`

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Ich versichere, dass ich diese Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

Heidelberg, 29. August 2018,

....

(signature)